ECEN-610: Mixed-Signal Interfaces

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ASSIGNMENT 6

Reconfigurable Low-Power Continuous-Time Sigma-Delta Converter for Multi-Standard Applications

1) Please use SIMULINK to design a continuous-time CT sigma-delta ADC (obtain specifications on modulator order, modulator topology, oversampling ratio (OSR), quantizer resolution) that can digitize a 200 KHz baseband signal at low-IF frequency of 100 KHz with 14 bits resolution. Please test your modulator using an input tone at frequency $f \leq f_b/3$, where $f_b = 200\,KHz$ for the Low-IF signal, so that to have the third harmonic of the output lying in the band of interest and hence get an actual measure of the achievable performance including the distortion. Provide a plot for the variation of the signal to noise plus distortion ratio (SNDR) versus the input signal amplitude and identify the achievable dynamic range (DR) on the plot. Note that the DR is defined by a lower limit at which the SNDR $= 0$ and its upper limit is the signal amplitude at which the SNDR drops from its maximum value by 6 dB. Figure 1 depicts an example for the SNDR variation vs. the input signal level and the resulting DR according to the above mentioned definition. Also, provide a plot for the output power spectrum using histograms (or FFT) for a -6dBFS input signal amplitude to show the noise shaping.

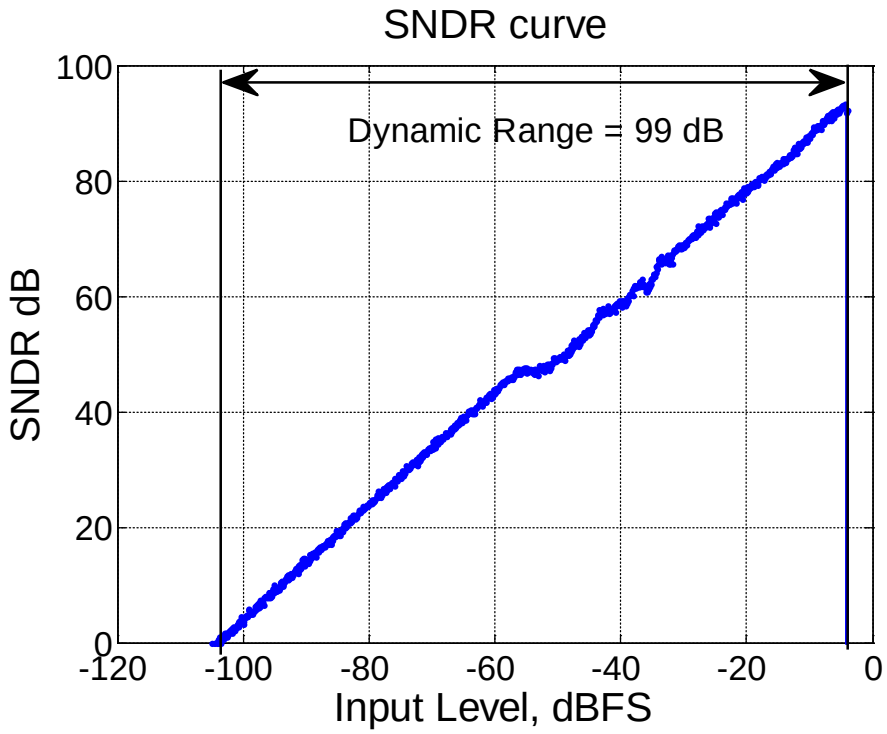

Fig. 1 SNDR Variation with Input Level

2) Using the systematic scaling scheme given in Fig. 2 [1], scale the feedforward and feedback coefficients of the modulator so that to account for the saturation limits at the output of the loop filter integrators. Consider saturation limits of ±0.9Vref, where Vref is the max, voltage level at the quantizer output. Repeat the plots required in the previous question, and compare between the two cases.

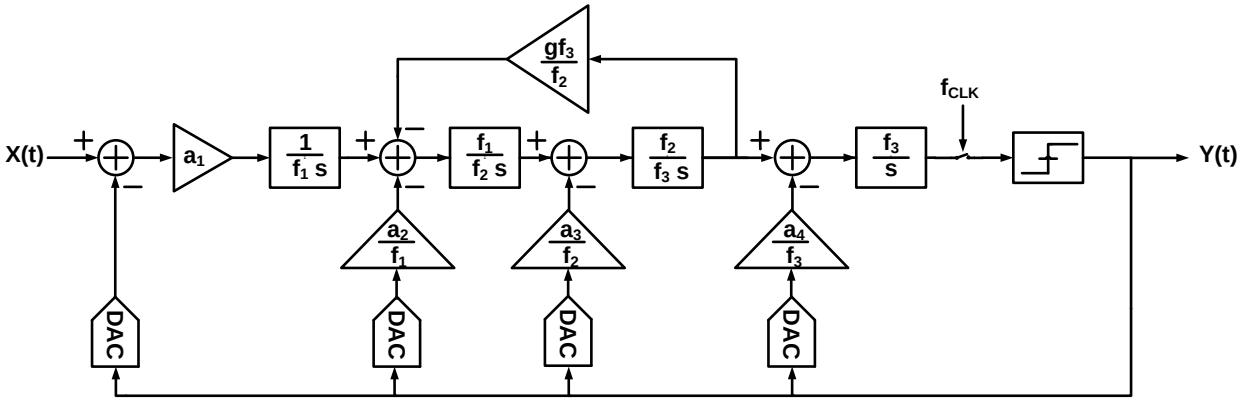

Fig. 2 Systematic scaling of loop coefficients

3) Include each of the following non-idealities within your Simulink model. Then, provide a plot showing the variation of SNDR versus each of the following non-idealities:

   a. Input Referred Thermal Noise.
   b. Jitter in Feedback DAC.
   c. Input Referred Total Harmonic Distortion (THD).
   d. Time-Constant (RC or Gm/C) variations.

4) Please make a convenient budget for each of the non-idealities mentioned in (3) so that the final dynamic range is 14 bits. Feel free to propose any solution that can remedy the effect of any of these non-idealities.

5) Nowadays there is an increasing interest in the industry to reduce the filtering used in the receiver chain so that to enable wide range of reconfigurability that can accommodate multi-standard receivers and future software-defined-radio receivers (SDRs). In this context, the filtering and anti-aliasing features associated with CT sigma-delta modulators need to be exploited as much as possible so that to relax requirements on the receive chain RF and baseband filtering. Figure 3 gives an example of a candidate topology for reconfigurable multi-standard receivers. In this receiver, the LNA is added after the antenna so that to attenuate the input referred noise contributed from the following receiver blocks, followed by the mixer to make direct (or low-IF) down-conversion of the channel of interest from RF to baseband frequencies. After the mixer, a tunable single-pole filtering is offered by a simple passive (highly linear) RC filter and then the

variable gain amplifier (VGA) is used to adjust the signal level to the input dynamic range of the CT $\Delta\sum$ modulator so that to avoid ADC overload and achieve the maximum possible SNDR.

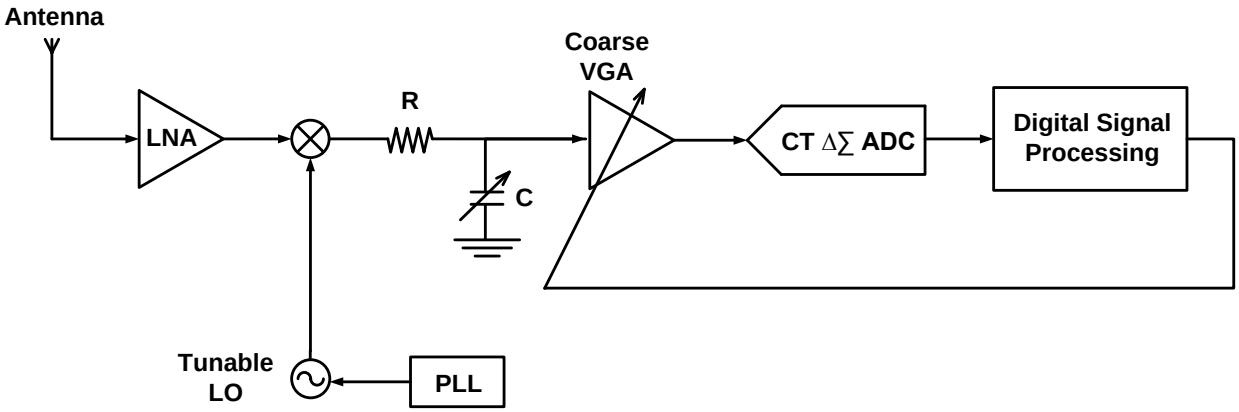

Fig. 3 Reconfigurable Multi-standard Receiver Topology

For example, consider the in-band blocking profile of the GSM standard shown in Fig. 4. The receiver should be able to detect a desired signal of -99 dBm in presence of in-band blockers with given strengths at the different bands included in the figure, while providing an SNR of at least 25 dB. After down-conversion to 100 KHz low-IF, the blocking profile will be as shown in Fig. 5. Please note that the negative spectrum image is not included and it will be removed in digital domain by virtue of orthogonal I/Q down-conversion, so we don't consider its effect in our analysis for simplicity. The only filtering that will be offered in the baseband is the first-order RC filtering either added explicitly or provided inherently by the trans-impedance amplifier (TIA) after the mixer. The main limitation against achieving the required resolution in presence of these blockers is due to the linearity of the ADC especially the first stage of the loop filter. Blockers cause desensitization of the amplifiers reducing the gain significantly in the band of interest and hence deteriorate the noise shaping and loop inherent anti-aliasing. Also, note that the power of the blockers is not increasing proportionally with the power of the input signal. That is, as the signal power increases, the power of the blockers stays the same. The blockers shown in Fig. 4 and Fig. 5 are the maximum possible blockers and they are assumed to be present with lowest signal power.

Please repeat the design and budgeting in question 4 for the ADC to accommodate these blockers and achieve a DR of 61 dB. Include the blockers (after being down-converted by the mixer and filter by a first order RC filter before the modulator) in your simulations and provide the resulting plots. You can add extra RC filtering before the modulator to improve the performance, if needed. Note that in this case the DR is defined as the range of the input signal amplitude for which the SNDR is $\geq$ 25 dB. Note also, that the amplitude of the blockers is determined by the ratio between their power and the power of the minimum detectable signal shown in Fig. 4 and Fig. 5, where the minimum detectable signal amplitude is defined as the first signal amplitude at which an SNDR

of ≥ 25 dB can be achieved. For higher signal amplitudes, the blockers should remain the same. That is, when simulating the modulator SNDR for different input signal amplitudes to determine the DR, the amplitudes of the blockers should increase linearly with the input signal, according to the ratios depicted in Fig. 4 and Fig. 5, until the minimum detectable signal is determined (for which SNDR ≥ 25 dB). After that, the blockers magnitudes should remain constant whereas the input signal magnitude should continue to increase during simulating the variation of the achievable SNDR versus the signal amplitude.

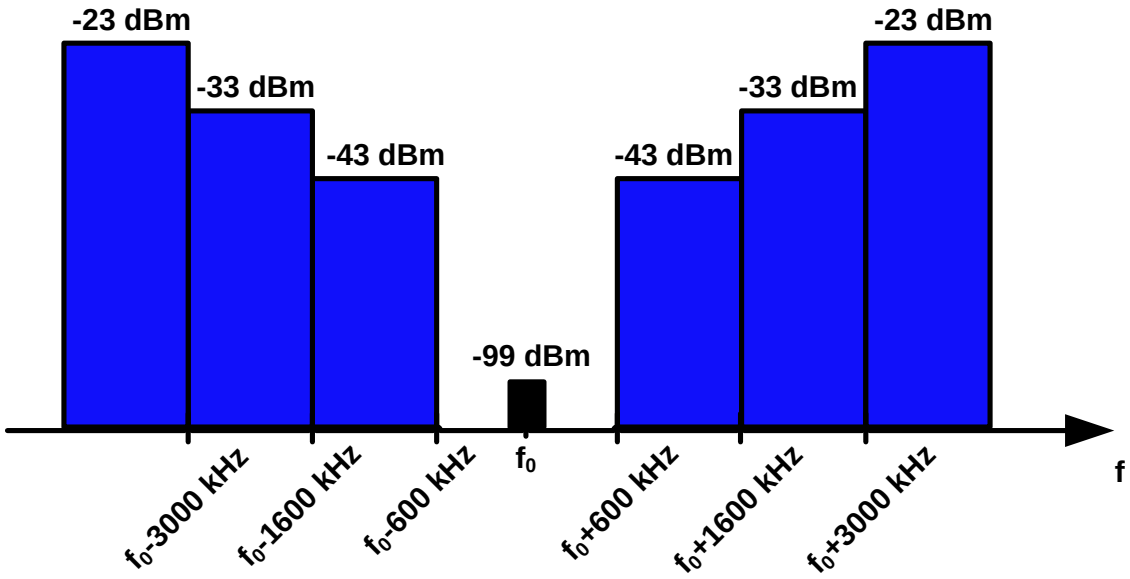

Fig. 4 GSM Blocking Profile

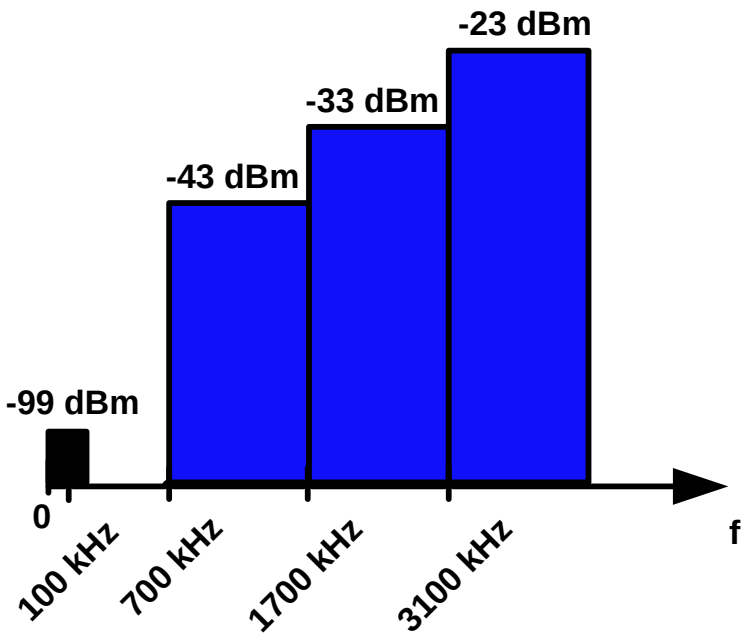

Fig. 5 After the mixer

References:

[1] N. Beilleau, H. Aboushady, and M.-M. Louerat. "Systematic Approach for Scaling Coefficients of Continuous-Time Sigma-Delta Modulators". MWSCAS, Dec. 2003.

[2] R. Ahmed, D.L. Aristizabal-Ramirez, and S. Hoyos, **"Sensitivity Analysis of Continuous-Time Delta-Sigma ADCs to Out-of-Band Blockers in Future SAW-Less Multi-Standard Wireless Receivers,"** *IEEE Transactions on Circuits and Systems I,* Vol. 59, No. 9, pp. 1894-1905, Sept. 2012.

[3] R. Saad, S. Hoyos and S. Palermo, "Analysis and Modeling of Clock-Jitter Effects in Delta-Sigma Modulators," book chapter in **"**MATLAB - A Fundamental Tool for Scientific Computing and Engineering Applications - Volume 1" edited by Vasilios N. Katsikis, ISBN 978-953-51-0750-7, Publisher: InTech, September 26, 2012.