

ECEN-610: Mixed-Signal Interfaces

Instructor: Sebastian Hoyos

ASSIGNMENT 5

LMS Calibration of Pipeline ADC

The project consists of modeling of a pipeline ADC using Simulink and then calibrating it using the LMS calibration method. The pipeline ADC to be modeled is a 500MHz; 13b with six stages each consisting of an MDAC with 2.5b resolution. Assume $V_{FS} = 1V$.

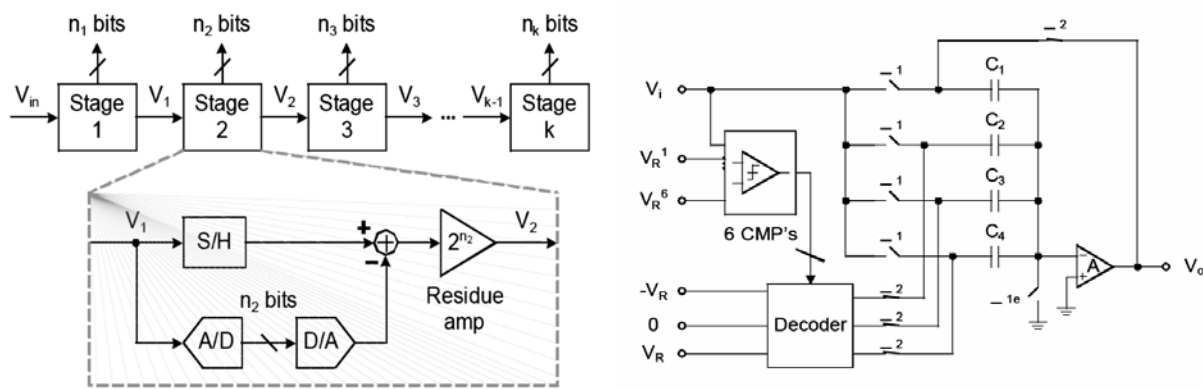


Figure 1: (a) General Pipeline Architecture

(b) 2.5b MDAC

1. Create a simulink model of the ADC. Model the individual MDAC stage from its ideal transfer function and then cascade the same block. Drive the ADC using an ideal tone of 200MHz frequency. Find out the SNR at the output. Comment on the result.
2. Introduce the following static errors in your MDAC model
 - Finite OTA Gain
 - OTA Offset
 - Capacitor Mismatch
 - Comparator Offset
 - Non-linear Op-Amp Open Loop Gain
 - Finite Op-Amp Bandwidth.

Find out the SNDR at the ADC output for several values of the mismatch introduced for each stage in each of these errors. Simulate each error individually and find the value of the error needed to degrade the SNDR to 10 dB.

All the static errors should be easily edited in a Matlab initialization file. The model should be able to generate performance plots for a given set of static errors. Your simulink model will be tested in the lab by the instructor with a pre-defined set of static errors.

- Use LMS algorithm to calibrate [1-4] for the static errors introduced in 2. The correction scheme for the Pipeline is given in the figure below,

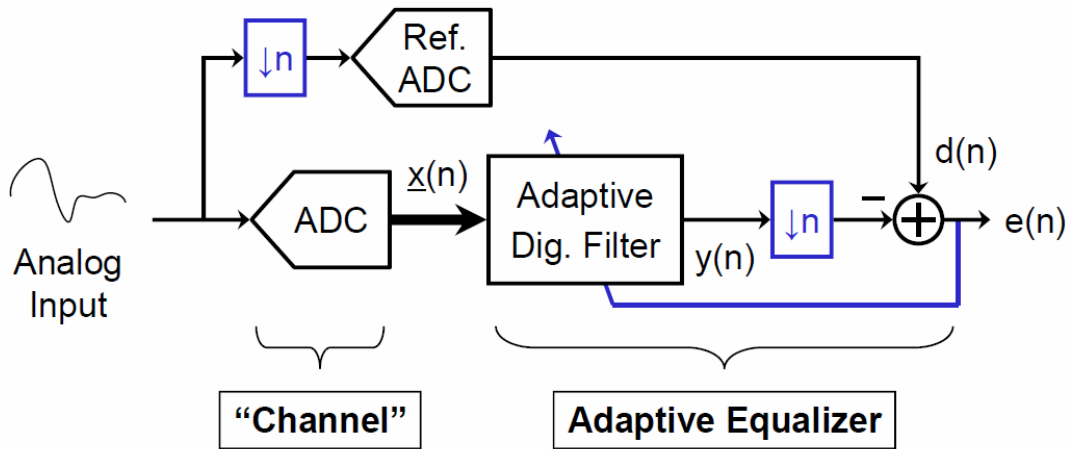


Figure 2: LMS Calibration Scheme for the ADC

The reference ADC can be assumed to be an ideal 16b ADC. The downsampling can be ignored. For example, the figure below shows the scheme for calibration of first four stages,

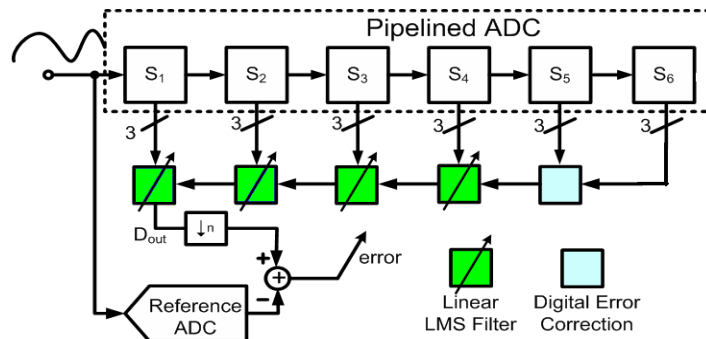


Figure 3: Calibration of first four stages

Give the number of stages calibrated and the number of parameters (weights) required to calibrate each stage. Study the convergence behaviour the LMS filter by plotting the error and weights. Find out the total number of iterations required for the SNR to reach the quantization limit. Comment of the relationship between step-size parameter (μ), speed of convergence and steady state error. Give the values of the final converged weights and compare them with the ideal weights.

4. Now, use Normalized LMS algorithm [5] to calibrate the same ADC. Study the convergence behaviour. Find out the number of iterations needed for convergence and compare with that of 3.
5. Now add noise to the ideal input tone of 200MHz so that the SNR is 80dB. The Op-Amp gain-bandwidth product is just 80% of the one needed to achieve 13b of resolution at $F_s=500$ MS/s. The open-loop gain has a second order non-linearity that is 10% of open-loop gain, a third order non-linearity that is 20% of the open-loop gain, a fourth order non-linearity that is 15% of the open-loop gain and a fifth order non-linearity that is 10% of the open-loop gain. Study the convergence behaviour of the LMS algorithm when up to the fifth order term is included in the calibration and comment on the results. Comment on the convergence of the algorithm for several decimations factors n (10, 100, 1000, 10000).
6. Derive an expression of the output of the ADC that includes all the non-idealities. Try to come up with a mathematical explanation of the convergence of the non-linear LMS algorithm for this application.
7. Drive the ADC with a full-scale multitone signal with bandwidth 200 MHz and 128 tones. The tones are modulated using BPSK modulation. Use the DFT to estimate the BPSK symbols. Without errors in the ADC, the DFT should lead to perfect estimates of the symbols. With errors in the ADC, the LMS will need to converge first before the DFT is applied. Analyze the convergence of the ADC when the ADC has only linear errors (Finite OTA Gain, OTA Offset, Capacitor Mismatch, Comparator Offset). Then include the non-linearities and repeat the simulations. Comment on the convergence of the algorithm for both cases for several decimations factors n (10, 100, 1000, 10000). Assume that the DFT and the multi-tone signal are perfectly synchronized. Please design the number of DFT points so the frequency bins lay exactly on the modulated tones. Calculate the MSE and BER in every case.

References

- [1] “*Background ADC Calibration in Digital Domain*”, Cheongyuen Tsang, Yun Chiu, Johan Vanderhaegen, Sebastian Hoyos, Charles Chen, Robert Brodersen, Borivoje Nikolic. CICC 2008, San Jose, CA
- [3] “*Background Digital Error Correction Technique for Pipelined Analog-Digital Converters*”, Sameer R. Sonkusale and Jan Van der Spiegel
- [4] “*Digital Background Calibration Technique for Pipeline ADCs with Multi-bit Stages*”, Antonio J. Ginés, Eduardo J. Peralías and Adoración Rueda
Proceedings of the 16th Symposium on Integrated Circuits and Systems Design (SBCCI'03)
- [5] “*An 8-bit 80-Msample/s Pipelined Analog-to-Digital Converter with Background Calibration*” Jun Ming, Member, IEEE, and Stephen H. Lewis, Fellow, IEEE IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 10, OCTOBER 2001
- [5] S. Haykin. *Adaptive Filter Theory*, Prentice Hall, 1986.