ECEN474: (Analog) VLSI Circuit Design
Fall 2011

Lecture 7: Table-Based (g_m/I_D) Design

Sebastian Hoyos
Analog & Mixed-Signal Center
Texas A&M University

Announcements

- Reading
  - Will post g_m/I_D paper
    - Material is only supplementary reference
- HW2 due Monday 9:10AM
- Exam 1 Friday Sept. 30

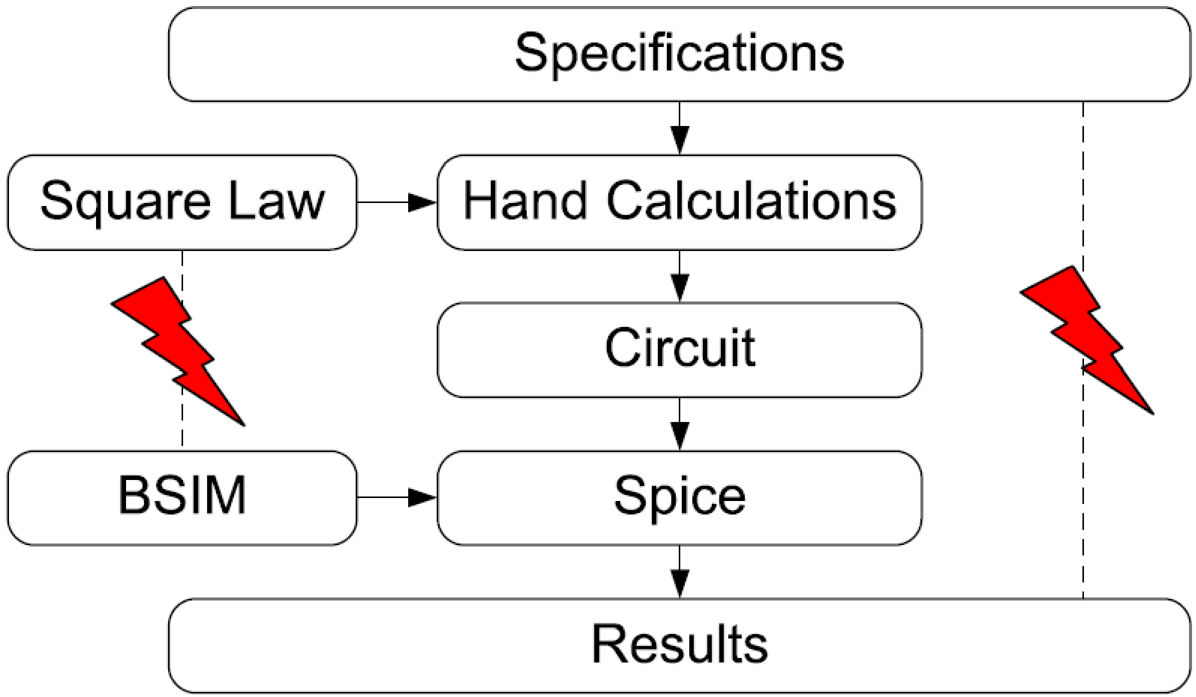
Agenda

- Technology characterization for design
- Table-based (g_m/I_D) design example
- Adapted from Prof. B. Murmann (Stanford) notes

How to Design with Modern Sub-Micron (Nanometer) Transistors?

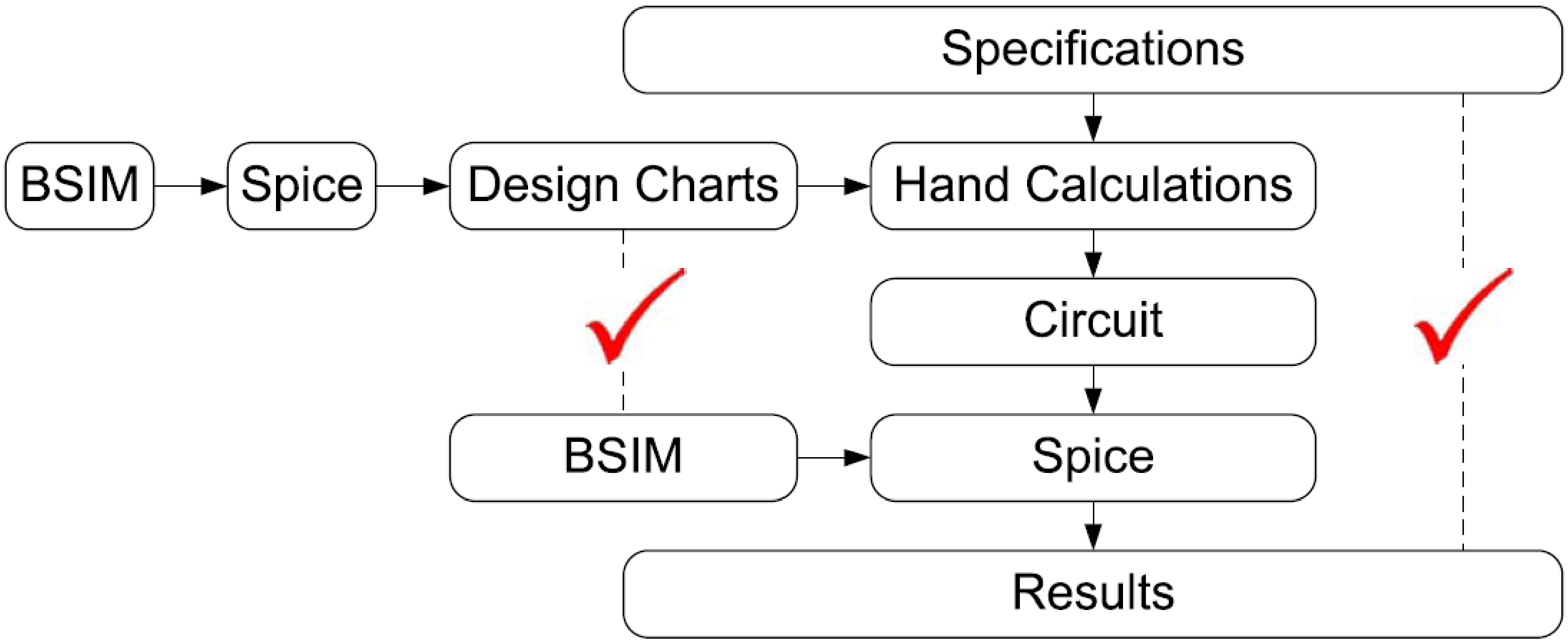
- Hand calculations with square-law model can deviate significantly from actual device performance
  - However, advanced model equations are too tedious for design
- Tempts designers to dive straight to simulation with little understanding on circuit performance trade-offs
  - “Spice Monkey” approach
- How can we accurately design when hand analysis models are way off?
- Employ a design methodology which leverages characterization data from BSIM simulations

The Problem



[Murmann]

The Solution

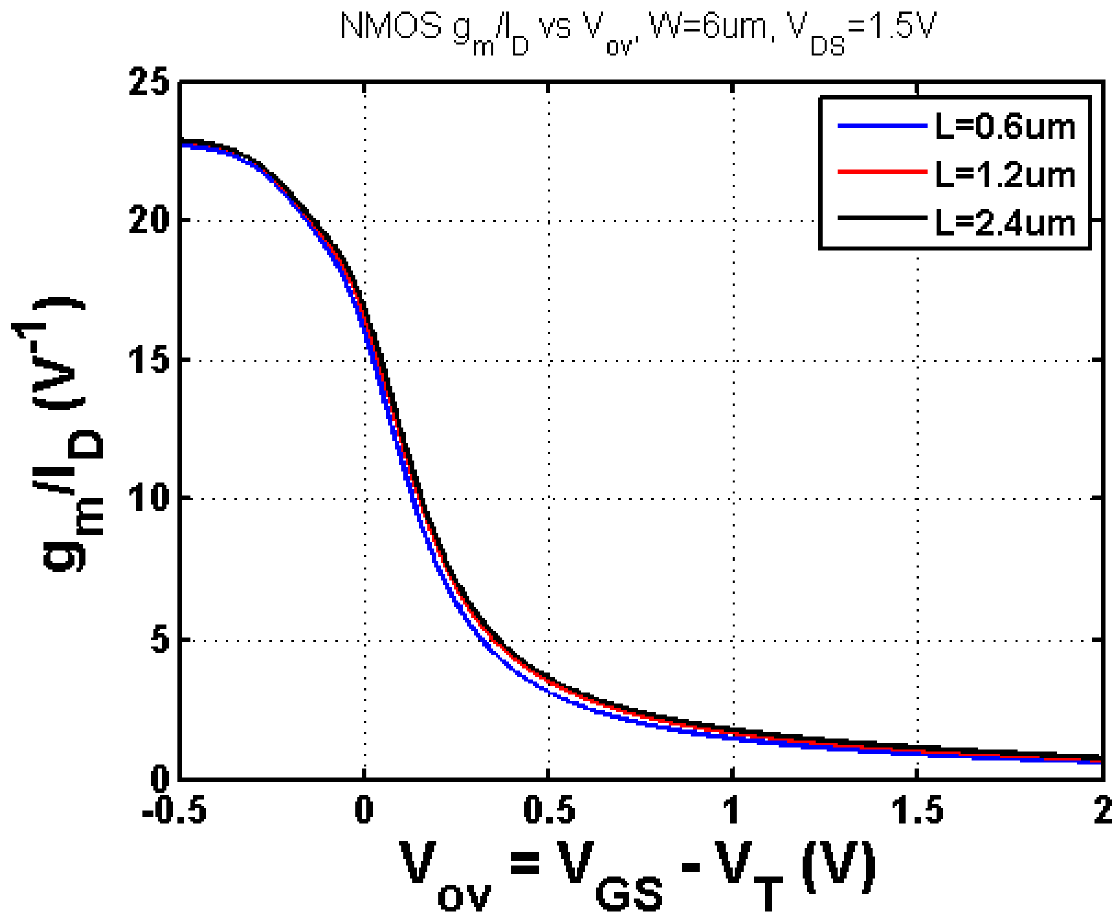


[Murmann]

Technology Characterization for Design

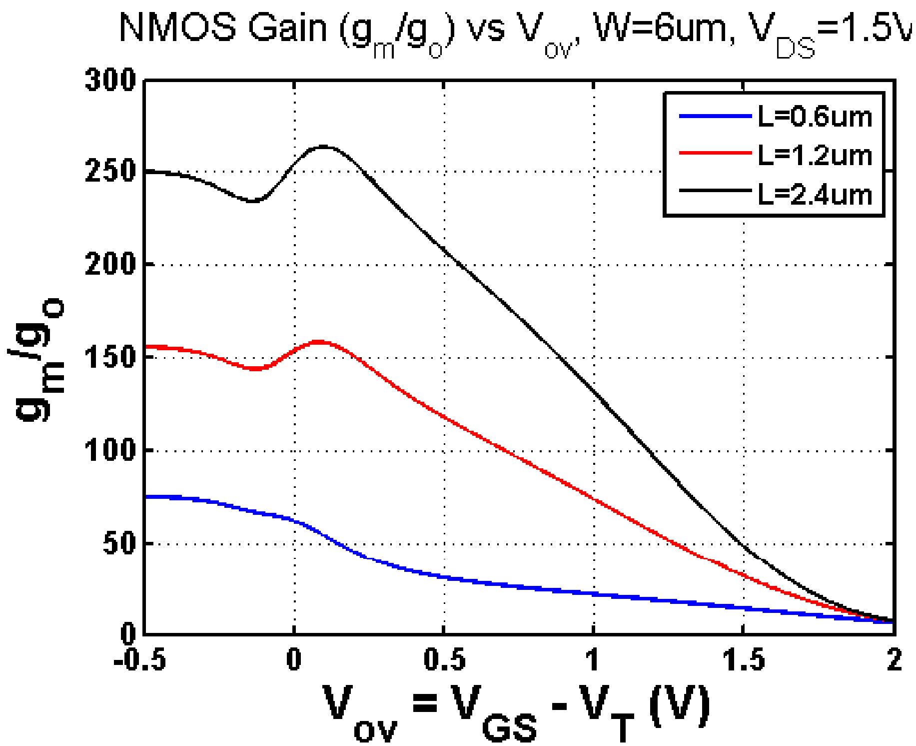
- Generate data for the following over a reasonable range of g_m/I_D and channel lengths
  - Transit frequency (f_T)
  - Intrinsic gain (g_m/g_{ds})
  - Current density (I_D/W)
- Also useful is extrinsic capacitor ratios
  - C_{gd}/C_{gg} and C_{dd}/C_{gg}
- Parameters are (to first order) independent of transistor width, which enables "normalized design"
- Do design hand calculations using the generated technology data
- Still need to understand how the circuit operates for an efficient design!!!

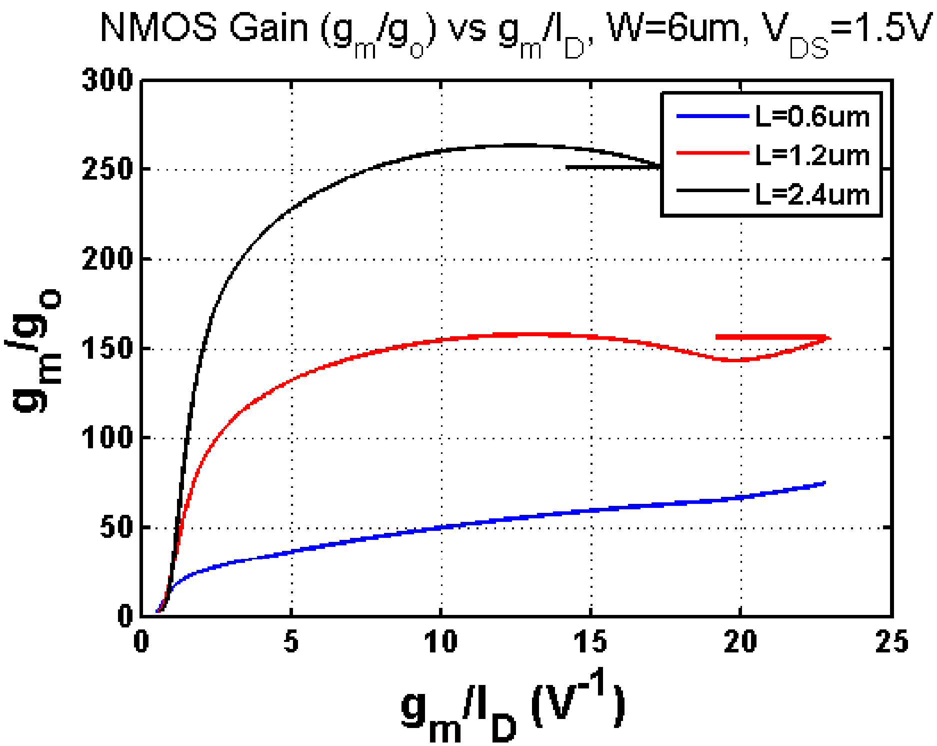
Gm/Id



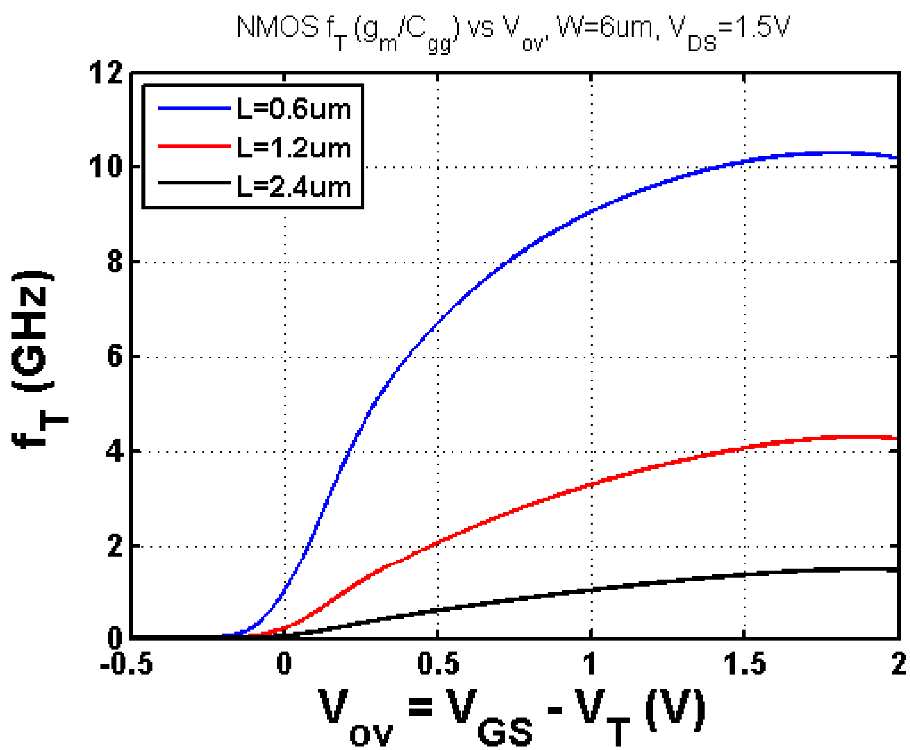
NMOS gm/ID vs Vov, W=6um, VDS=1.5V
L=0.6um
L=1.2um
L=2.4um
gm/ID (V-1)
Vov = VGS - VT (V)
25
20
15
10
5
0
-0.5
0
0.5
1
1.5
2

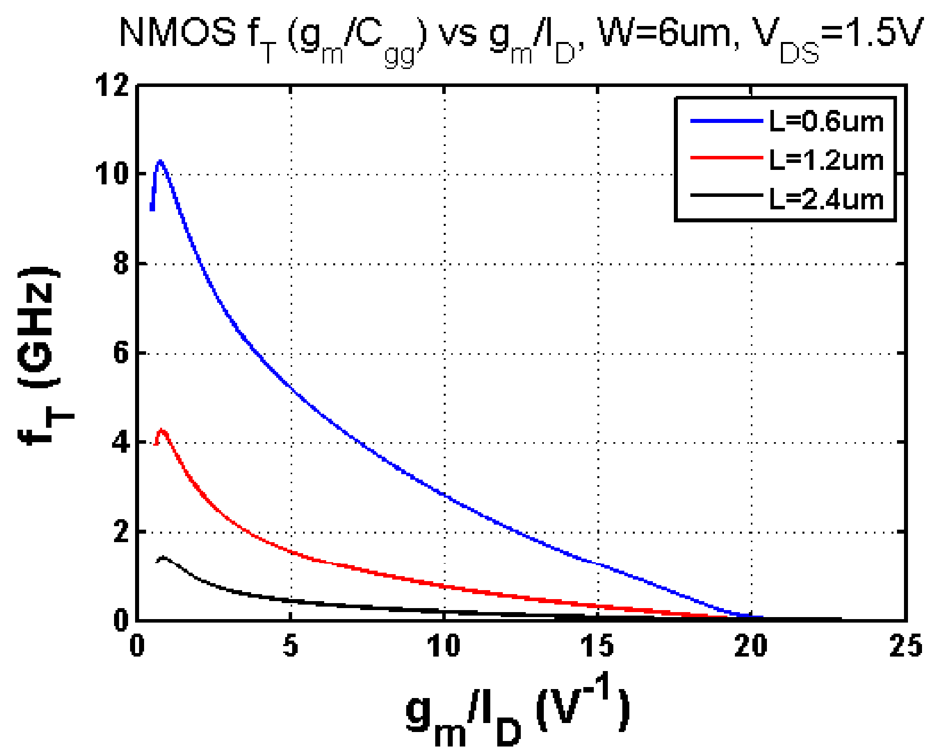
Gain


NMOS Gain (gm/go) vs Vov, W=6um, VDS=1.5V
L=0.6um
L=1.2um
L=2.4um
gm/go
Vov = VGS - VT (V)
300
250
200
150
100
50
0
-0.5
0
0.5
1
1.5
2

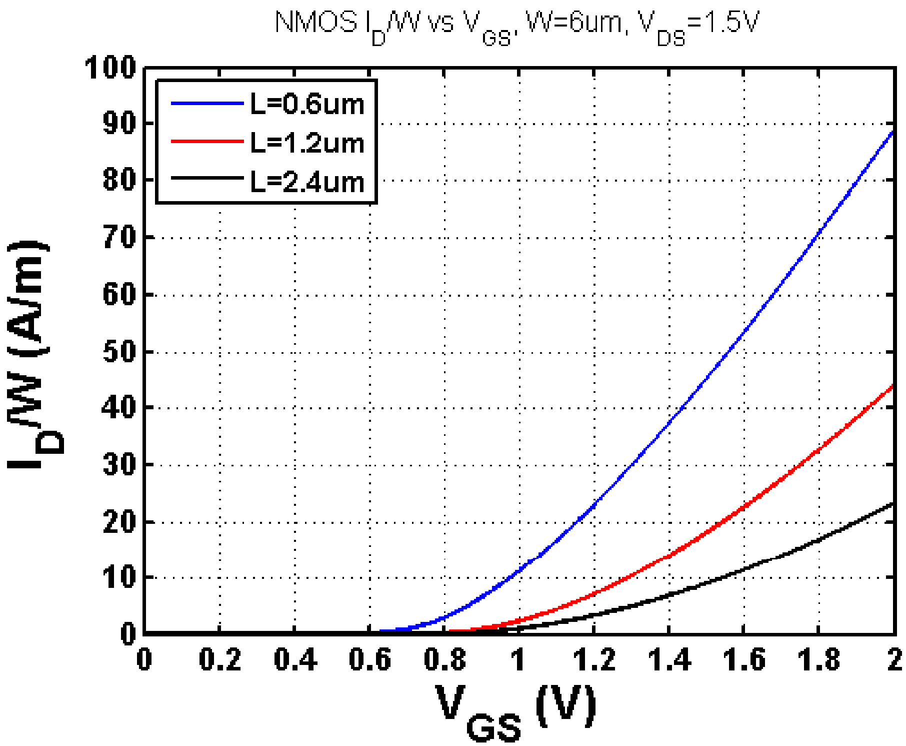

NMOS Gain (gm/go) vs gm/ID, W=6um, VDS=1.5V
L=0.6um
L=1.2um
L=2.4um
gm/go
gm/ID (V-1)
300
250
200
150
100
50
0
0
5
10
15
20
25

f_T

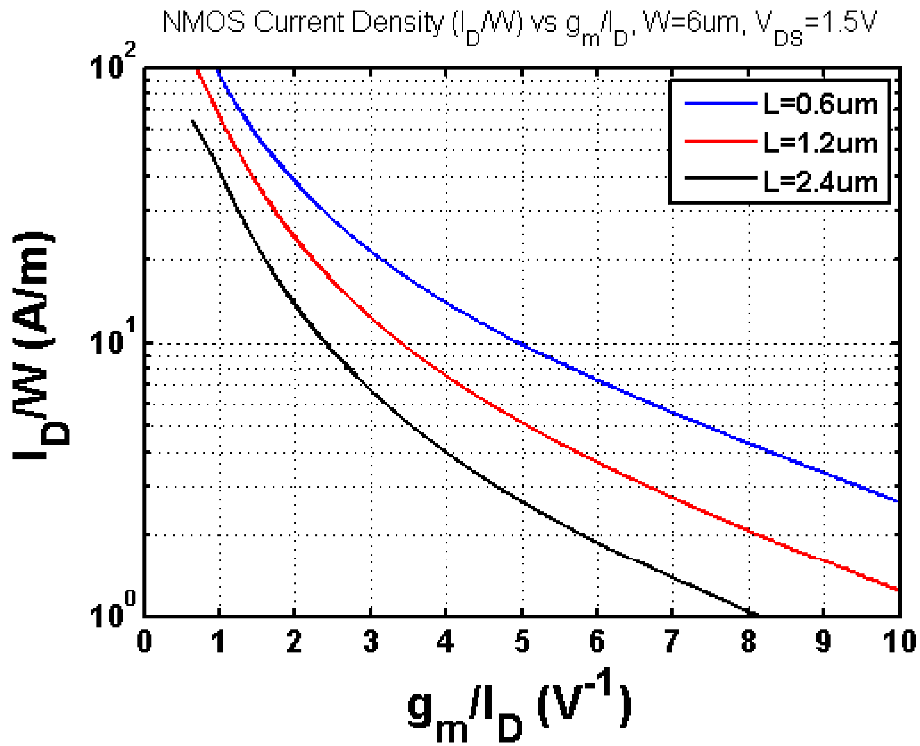

NMOS f_T (g_m/C_{gg}) vs V_{ov}, W=6um, V_{DS}=1.5V
L=0.6um
L=1.2um
L=2.4um
f_T (GHz)
$V_{ov} = V_{GS} - V_T$ (V)


NMOS f_T (g_m/C_{gg}) vs g_m/I_D, W=6um, V_{DS}=1.5V
L=0.6um
L=1.2um
L=2.4um
f_T (GHz)
g_m/I_D (V^{-1})

ID/W

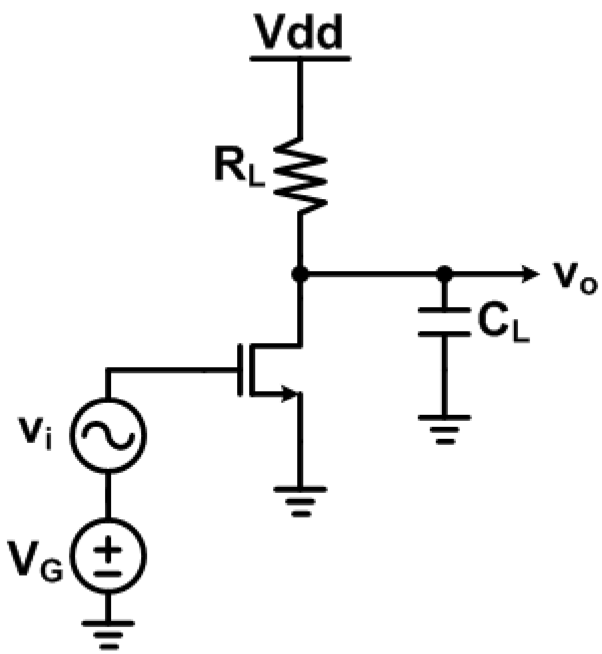


NMOS I_D/W vs V_{GS}, W=6um, V_{DS}=1.5V
L=0.6um
L=1.2um
L=2.4um
I_D/W (A/m)
V_{GS} (V)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70
80
90
100



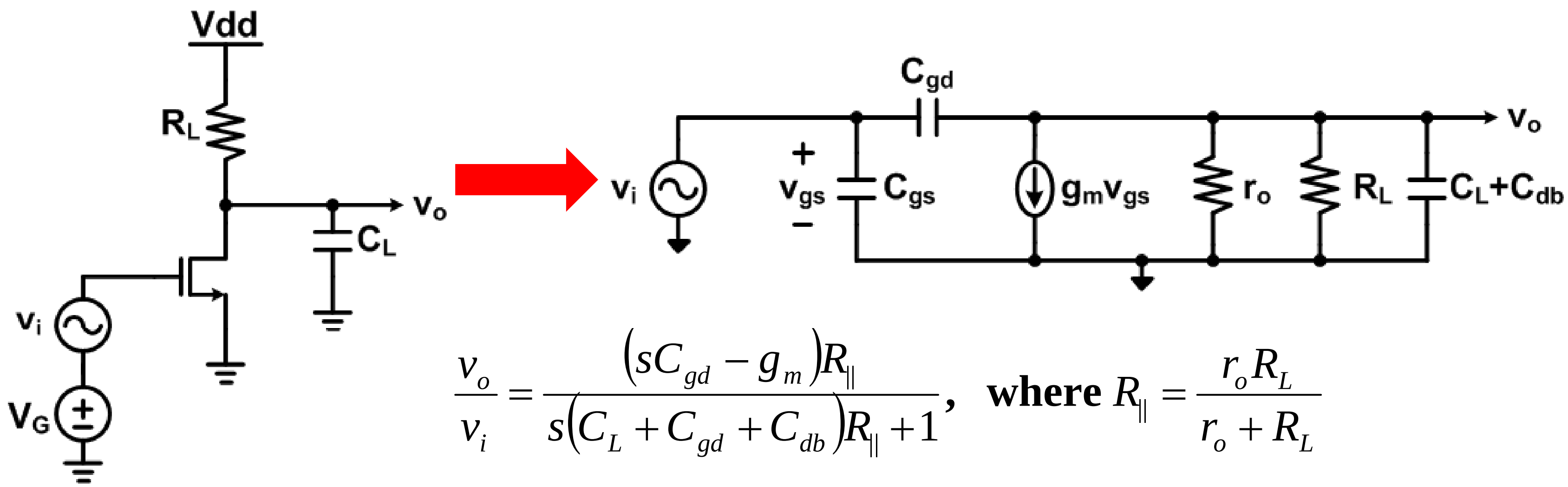
NMOS Current Density (I_D/W) vs g_m/I_D, W=6um, V_{DS}=1.5V
L=0.6um
L=1.2um
L=2.4um
I_D/W (A/m)
g_m/I_D (V^{-1})
10^0
10^1
10^2
0
1
2
3
4
5
6
7
8
9
10

CS Amplifier Design Example



- Specifications
  - 0.6μm technology
  - $|A_v| \geq 4V/V$
  - $f_u \geq 100MHz$
  - $C_L = 5pF$
  - Vdd = 3V

CS Amplifier Small-Signal Model (No R_S)



$$\frac{v_o}{v_i} = \frac{(sC_{gd} - g_m)R_{\|}}{s(C_L + C_{gd} + C_{db})R_{\|} + 1}, \quad \textbf{where } R_{\|} = \frac{r_o R_L}{r_o + R_L}$$

$$\omega_z = \frac{g_m}{C_{gd}} \quad \textbf{(located at very high frequency,} > \omega_{\mathbf{T}}\textbf{)}$$

$$\omega_p = -\frac{1}{R_{\|}(C_L + C_{gd} + C_{db})} \approx -\frac{1}{R_L C_L}$$

$$A_v = -g_m R_{\|} \approx -g_m R_L$$

$$\omega_u = A_v \omega_p \approx \frac{g_m}{C_L}$$

Design Procedure

1. Determine g_m from design specifications
   a. ω_u in this example
2. Pick transistor L
   a. Short channel $\rightarrow$ high f_T (high bandwidth)
   b. Long channel $\rightarrow$ high r_o (high gain)
3. Pick g_m/I_D (or f_T)
   a. Large $g_m/I_D \rightarrow$ low power, large signal swing (low V_{ov})
   b. Small $g_m/I_D \rightarrow$ high f_T (high speed)
   c. May also be set by common-mode considerations
4. Determine I_D/W from I_D/W vs g_m/I_D chart
5. Determine W from I_D/W

- Other approaches exist

1. Determine g_m (& R_L)

- From ω_u and DC gain specification

$$\omega_u = A_v \omega_p \approx \frac{g_m}{C_L}$$

$$g_m = \omega_u C_L = 2\pi(100MHz)(5pF) = 3.14mA/V$$

Note, this may be slightly low due to neglecting C_{gd} and C_{db}

$$A_v = -g_m R_{\|} \approx -g_m R_L$$

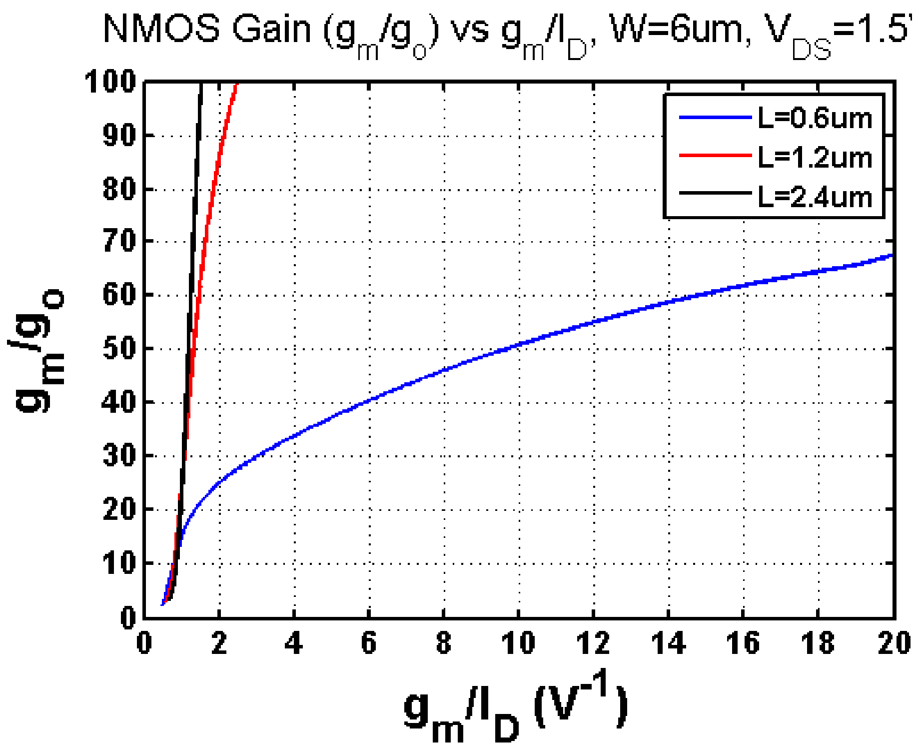
$$R_L = \frac{A_v}{g_m}$$

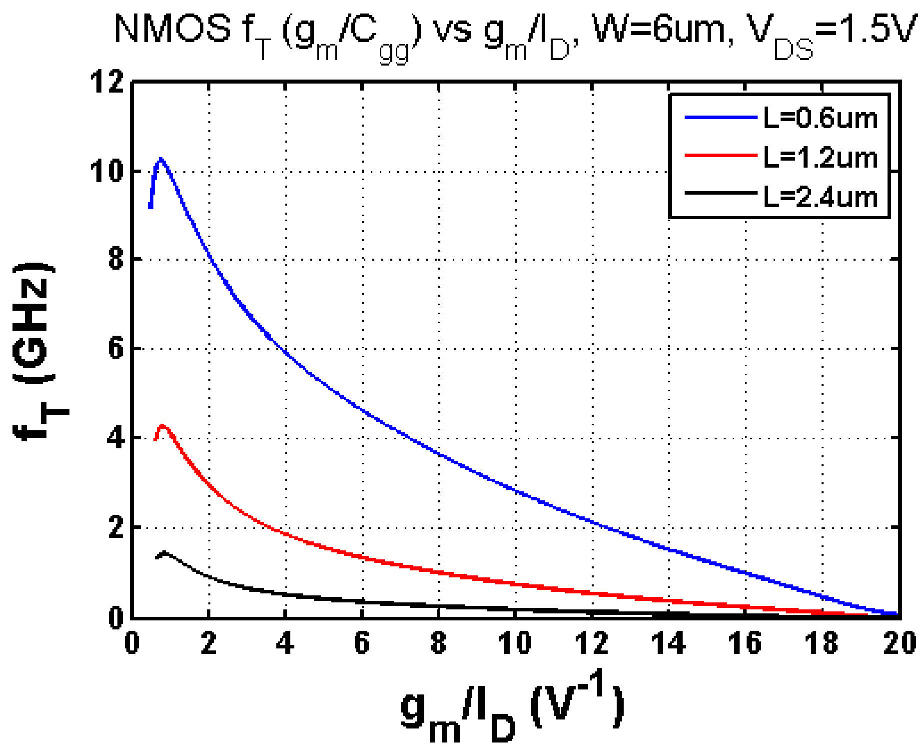
Adding 20% margin to compensate for r_o effects

$$R_L = \frac{A_v}{g_m} = \frac{4.8}{3.14mA/V} = 1.5k\Omega$$

2. Pick Transistor L

- Need to look at gain and f_T plots

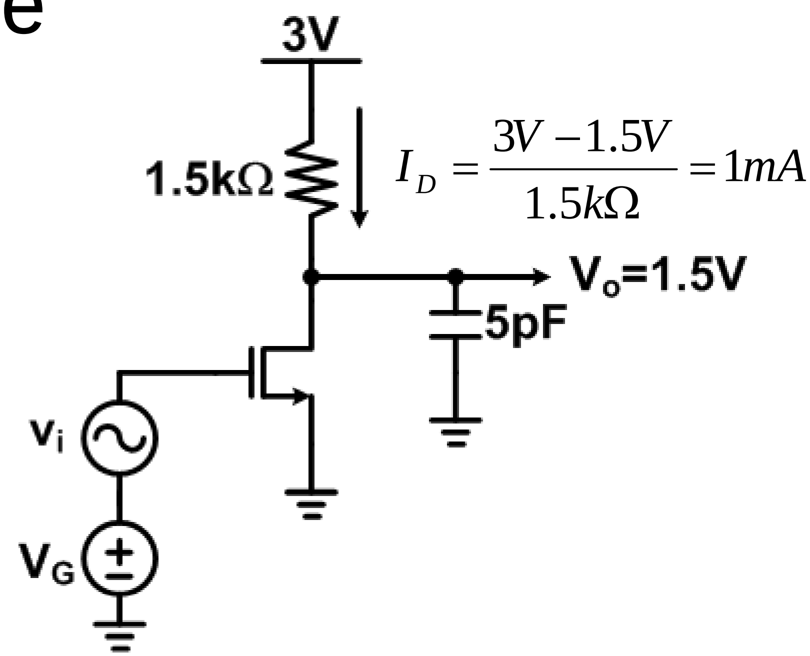




- Since amplifier $A_V \geq 4$, min channel length (L=0.6μm) will work with g_m/I_D~>2
  - Min channel length provides highest f_T at this g_m/I_D setting

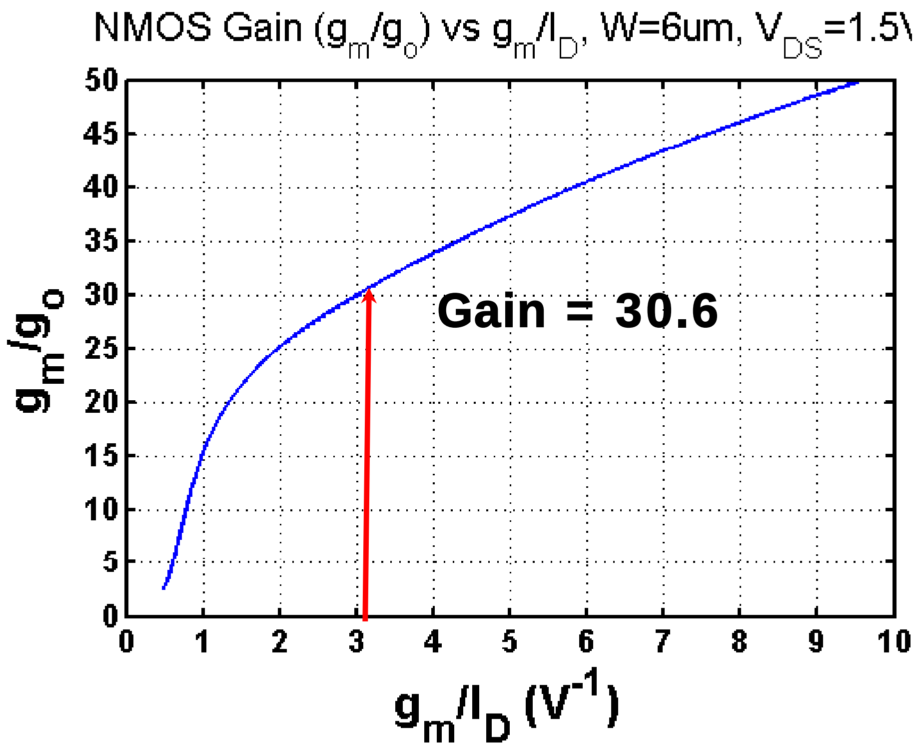
3. Pick g_m/I_D (or f_T)

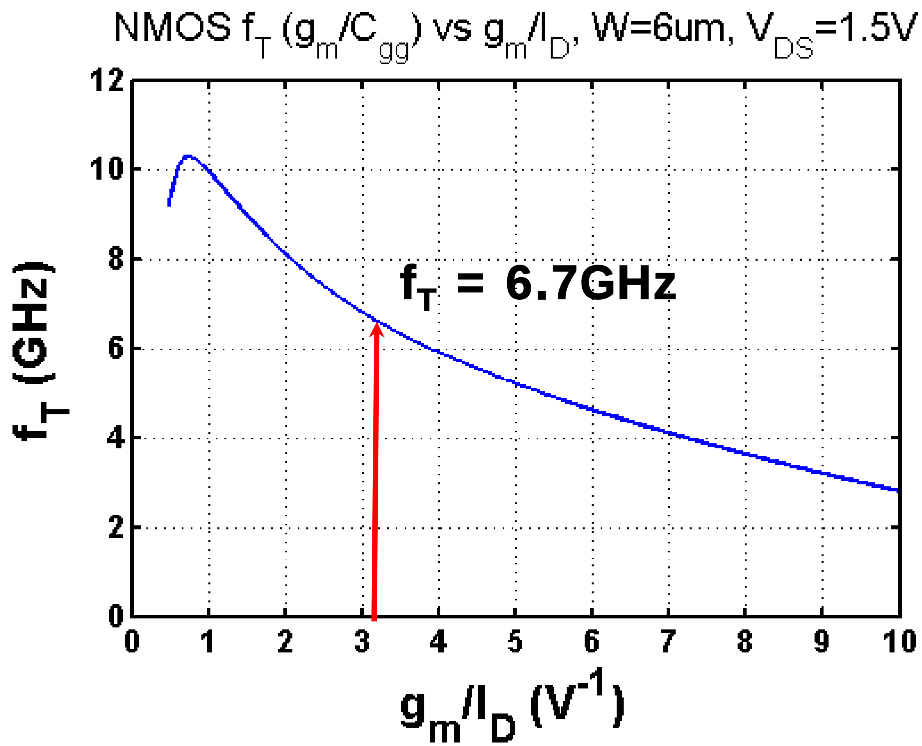
- Setting I_D for V_O=1.5V for large output swing range



$$\frac{g_m}{I_D} = \frac{3.14mA/V}{1mA} = 3.14V^{-1}$$

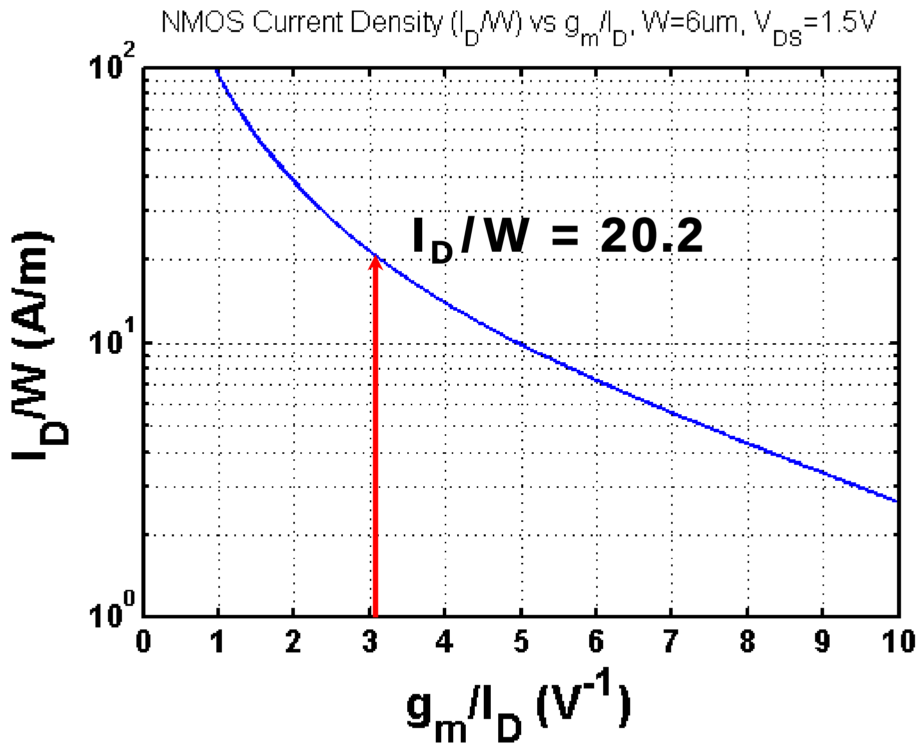
Verify Transistor Gain & f_T at g_m/I_D Setting

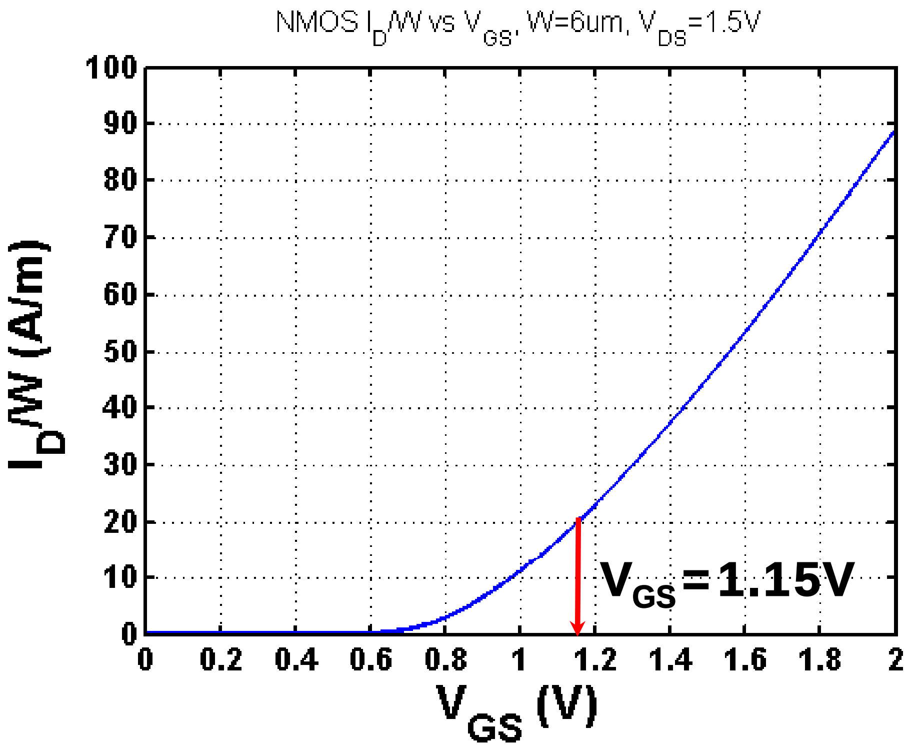




- Transistor gain=30.6 >> amplifier $A_V \geq 4$
- Transistor f_T=6.7GHz >> amplifier f_u=100MHz
- g_m/I_D setting is acceptable

4. Determine Current Density (I_D/W)





- $g_m/I_D=3.14V^{-1}$ maps to a current density of 20.2μA/μm

- Verify current density is achievable at a reasonable V_{GS}
- V_{GS}=1.15V is reasonable with Vdd=3V & V_{DS}=1.5V

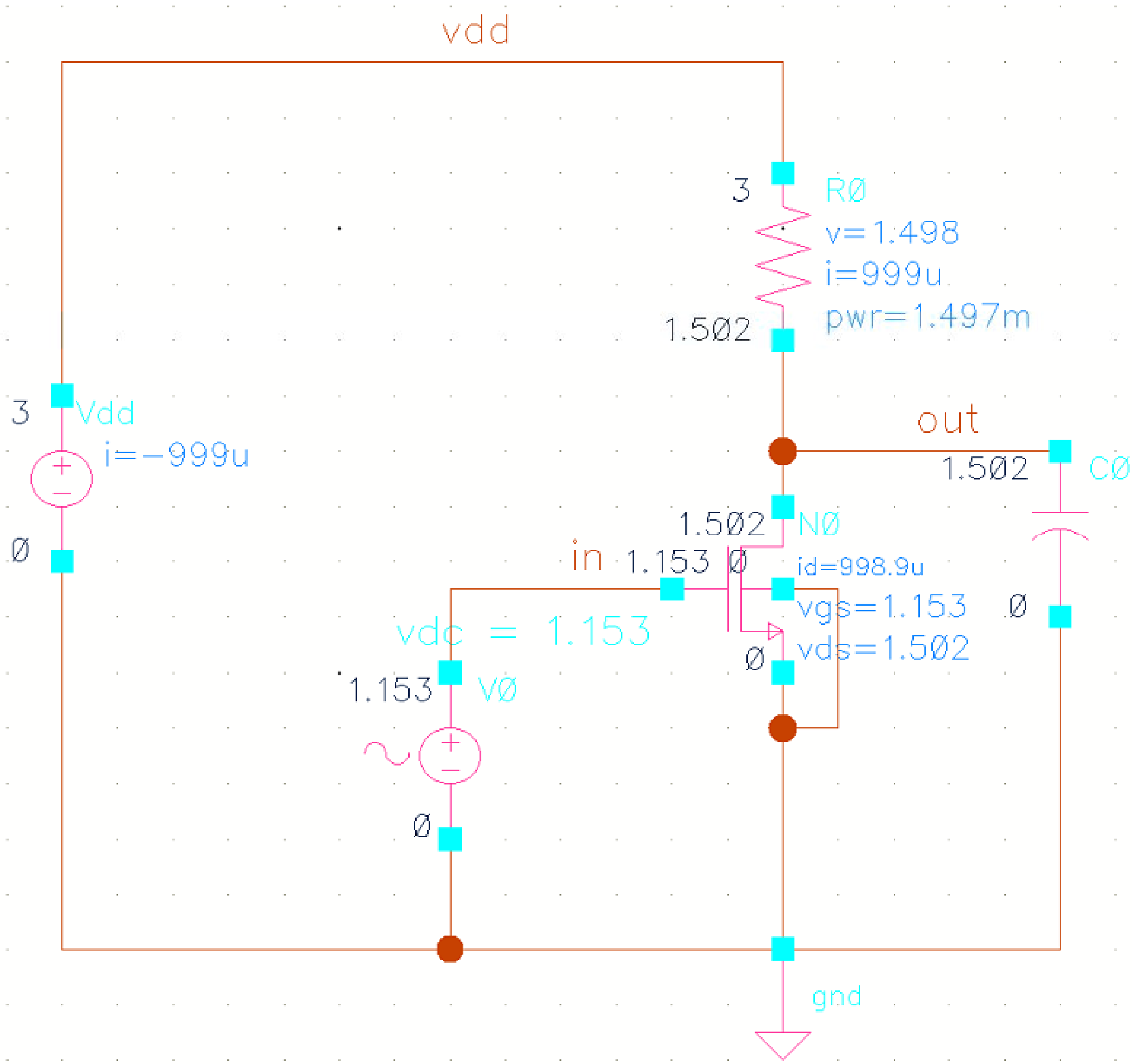
5. Determine Transistor W from I_D/W

- From Step 3, we determined that I_D=1mA

$$W = \frac{I_D}{\left(I_D/W\right)} = \frac{1mA}{20.2\mu A/\mu m} = 49.5\mu m$$

- For layout considerations and to comply with the technology design rules
  - Adjust 49.5μm to 49.2μm and realize with 8 fingers of 6.15μm
  - This should match our predictions well, as the charts are extracted with a 6μm device
    - Although it shouldn't be too sensitive to exact finger width

Simulation Circuit



Operating Point Information

Design Value

N0:betaeff	9.97E-03
N0:cbb	2.48E-14
N0:cbd	-1.28E-17
N0:cbdbi	5.56E-14
N0:cbg	-8.56E-15
N0:cbs	-1.63E-14
N0:cbsbi	-1.63E-14
N0:cdb	-4.26E-15
N0:cdd	1.25E-14
N0:cddbi	-5.56E-14
N0:cdg	-2.87E-14
N0:cds	2.05E-14
N0:cgb	-1.42E-14
N0:cgbovl	0
N0:cgd	-1.25E-14
N0:cgdbi	5.07E-17
N0:cgdovl	1.26E-14
N0:cgg	7.41E-14
N0:cggbi	4.90E-14
N0:cgs	-4.74E-14
N0:cgsbi	-3.49E-14
N0:cgsovl	1.26E-14
N0:cjd	5.56E-14
N0:cjs	0
N0:csb	-6.39E-15
N0:csd	-2.60E-17

N0:csg	-3.68E-14	
N0:css	4.32E-14	
N0:cssbi	3.07E-14	
N0:gbd	0	
N0:gbs	1.03E-10	
N0:gds	1.02E-04	
N0:gm	3.13E-03	3.14mA/V
N0:gmbs	7.64E-04	
N0:gmoverid	3.131	$3.14V^{-1}$
N0:i1	9.99E-04	
N0:i3	-9.99E-04	
N0:i4	-8.00E-14	
N0:ibd	-8.00E-14	
N0:ibs	0	
N0:ibulk	-8.00E-14	
N0:id	9.99E-04	1mA
N0:ids	9.99E-04	
N0:igb	0	
N0:igcd	0	
N0:igcs	0	
N0:igd	0	
N0:igidl	0	
N0:igisl	0	
N0:igs	0	
N0:is	-9.99E-04	
N0:isub	0	
N0:pwr	1.50E-03	

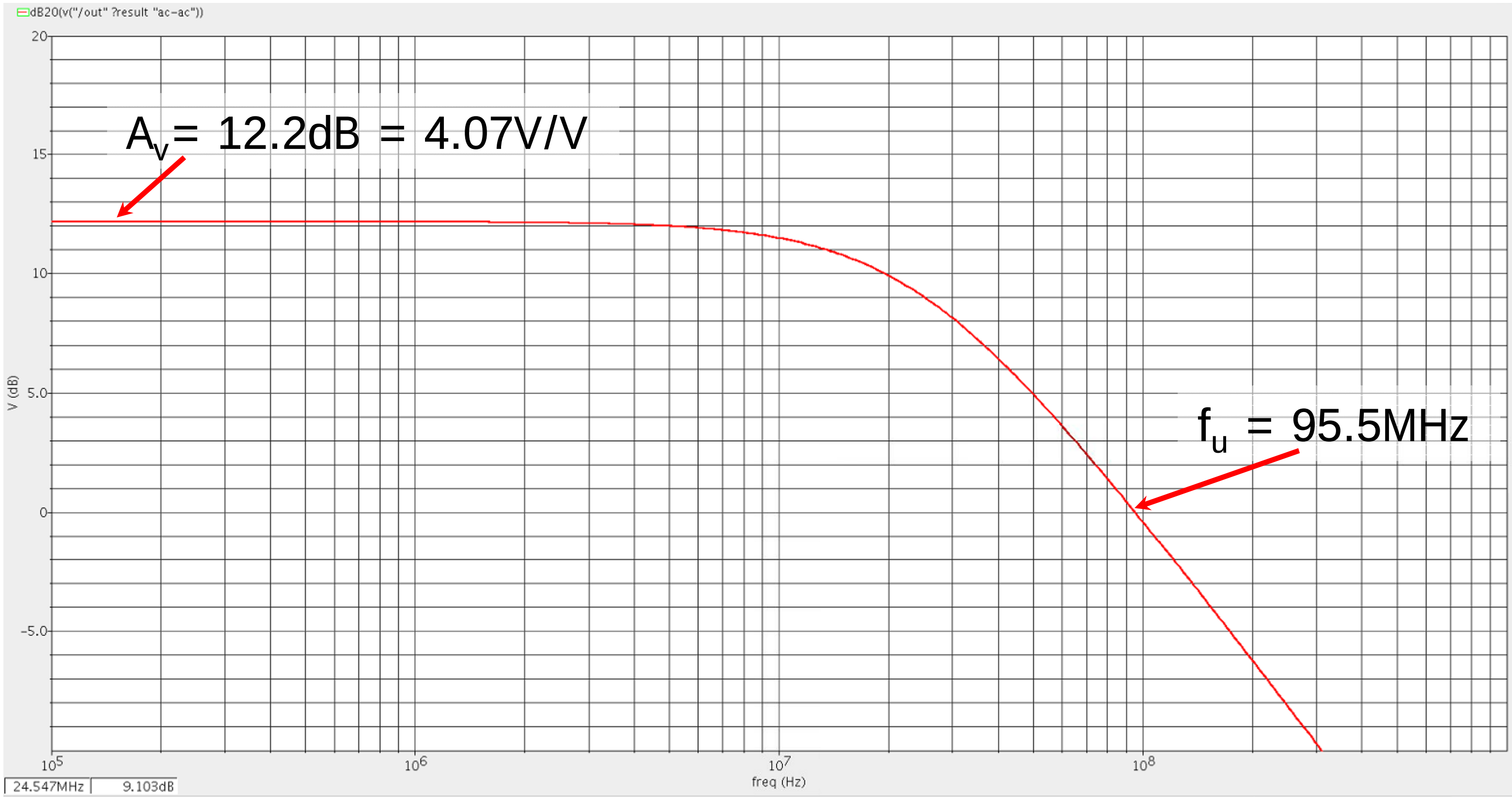
N0:qb	-5.03E-14
N0:qbd	-9.46E-14
N0:qbi	-5.03E-14
N0:qbs	0
N0:qd	-3.72E-15
N0:qdi	-8.10E-15
N0:qg	8.07E-14
N0:qgi	7.06E-14
N0:qinv	4.20E-03
N0:qsi	-1.21E-14
N0:qsrco	-2.66E-14
N0:region	2
N0:reversed	0
N0:ron	1.50E+03
N0:type	0
N0:vbs	0
N0:vdb	1.502
N0:vds	1.502
N0:vdsat	3.91E-01
N0:vfbeff	-9.65E-01
N0:vgb	1.153
N0:vgd	-3.49E-01
N0:vgs	1.153
N0:vgsteff	5.00E-01
N0:vth	6.53E-01

Total Cgate = Cgg = 74.1fF

Total Cdrain = Cdd + Cjd = 12.5fF + 55.6fF = 68.1fF

Total Csource = Css + Cjs = 43.2fF + 0fF = 43.2fF

AC Response



- Design is very close to specs
- Discrepancies come from neglecting r_o and C_{drain}
- With design table information we can include estimates of these in our original procedure for more accurate results

Next Time

- Current Mirrors