ECEN474: (Analog) VLSI Circuit Design
Fall 2011

Lecture 5: MOS Transistor Modeling

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Announcements

- Lab 1 this week
- Reading for next time
  - Razavi's CMOS book chapter 16

Agenda

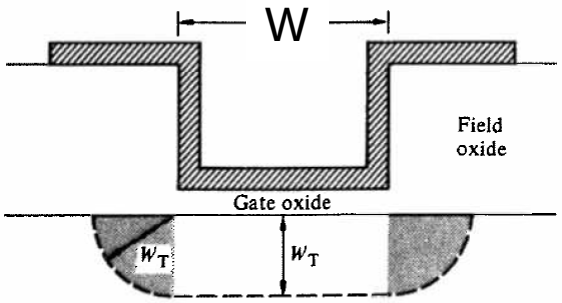
- Threshold voltage dependencies on W,L
- Temperature dependencies
- Process corners
- Technology characterization for design
  - Adapted from Prof. B. Murmann (Stanford) notes

V_T Dependency on W

- Gate-controlled depletion region extends in part outside the gate width
- V_T monotonically increases with decreasing channel width

$$V_T = V_{Twide} + \Delta V_T$$

$$\Delta V_T = \frac{qN_A W_T}{C_{ox}} \frac{\pi W_T}{2W}$$



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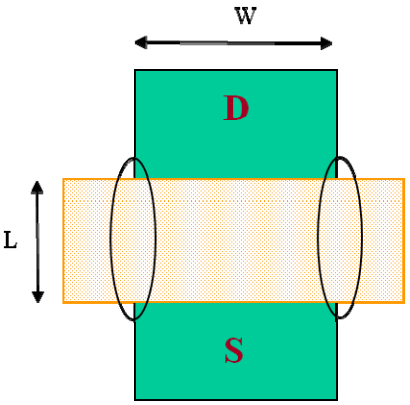
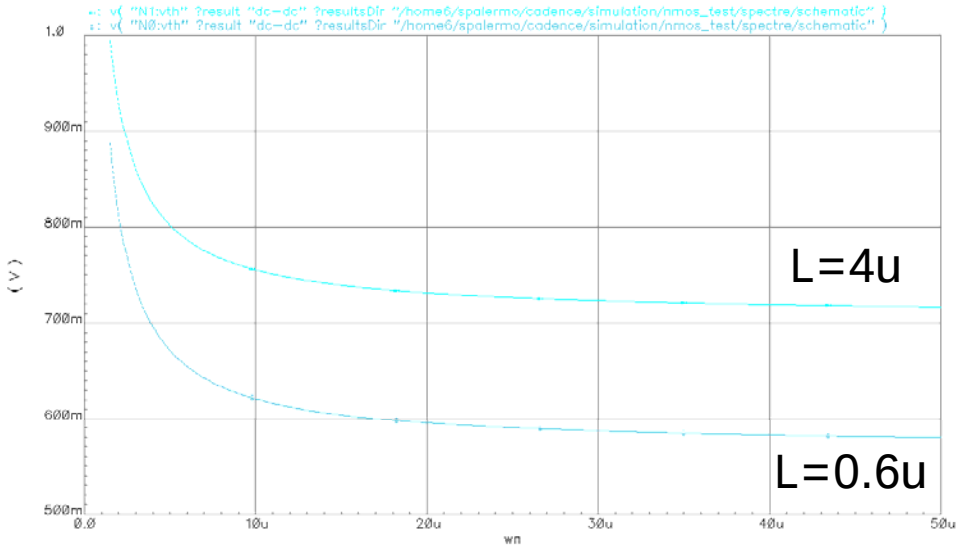
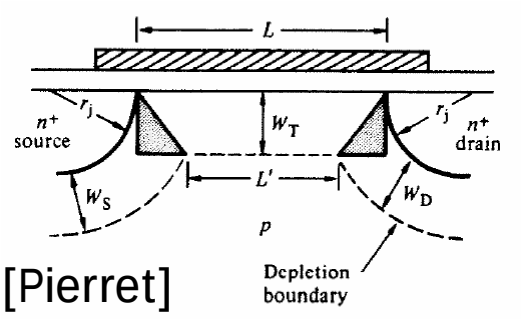




V_T Dependency on L

- Source and drain assist in forming the depletion region under the gate

- With simple model, V_T monotonically decreases with decreasing channel length



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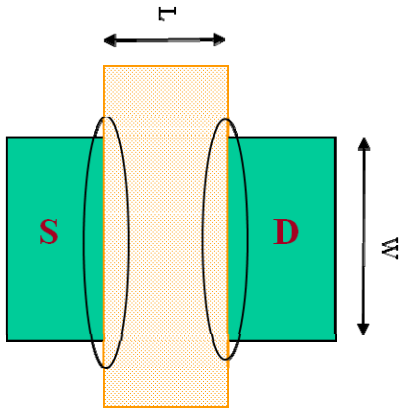
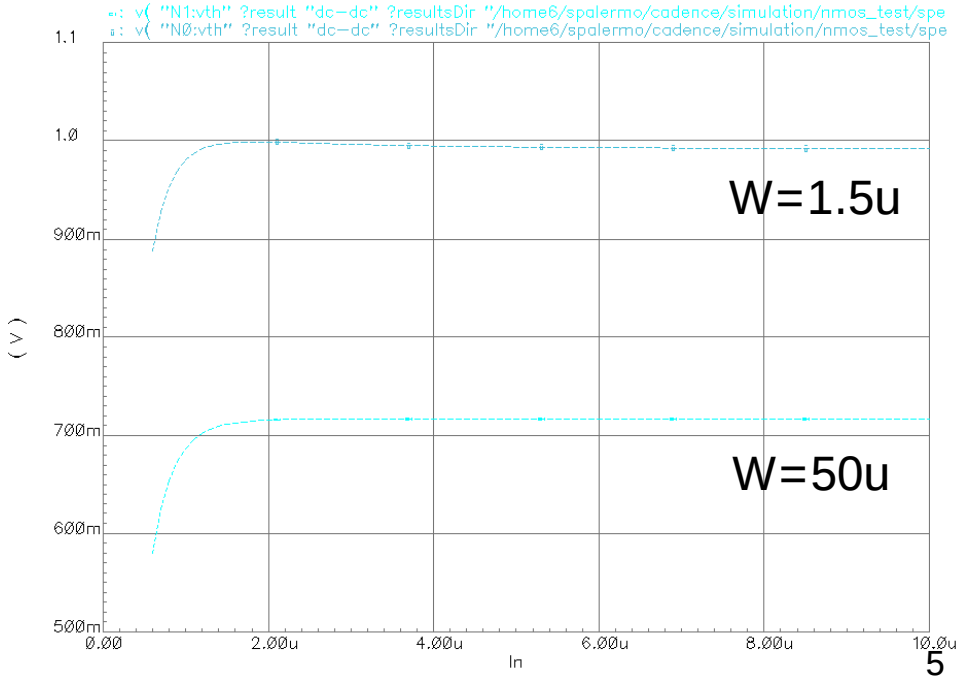


$$V_T = V_{Tlong} + \Delta V_T$$

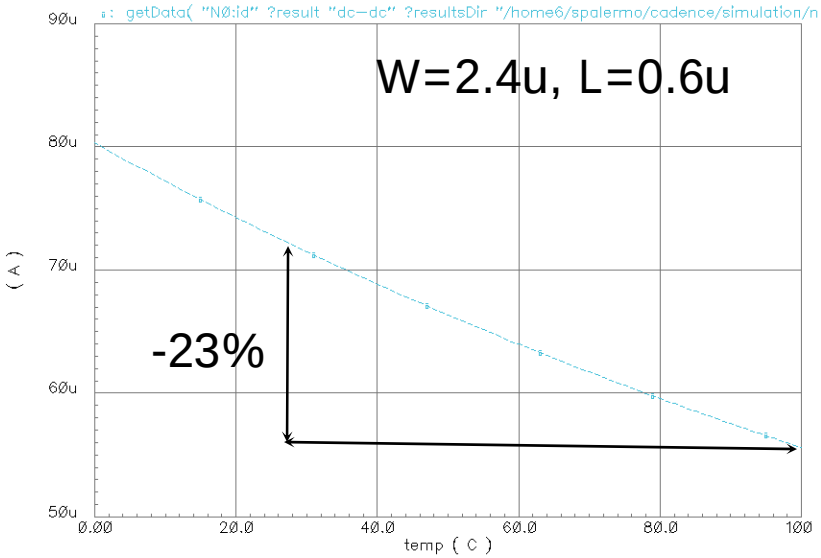
$$\Delta V_T = -\frac{qN_A W_T}{C_{ox}} \frac{r_j}{L}\left(\sqrt{1+\frac{2W_T}{r_j}} - 1\right)$$



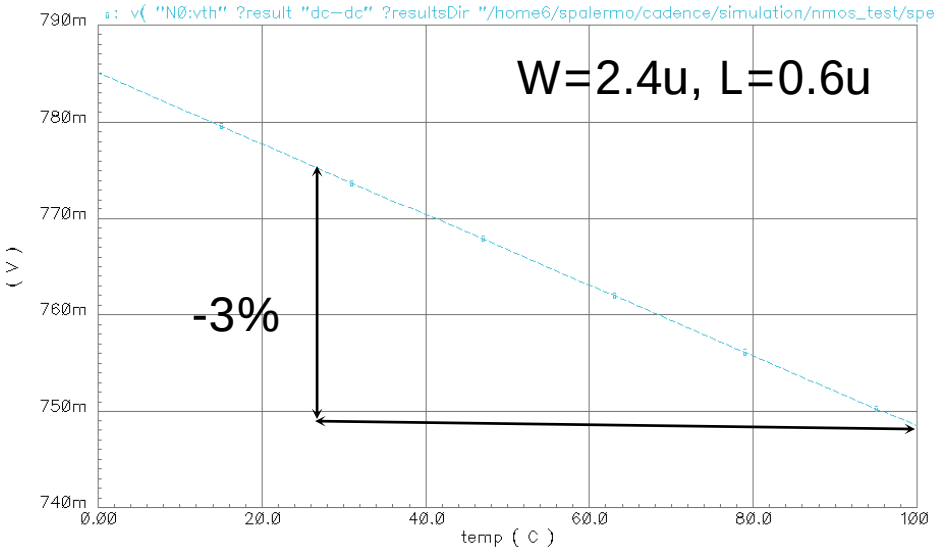
Temperature Dependence

- Transistor mobility and threshold voltage are dependent on temperature
  - Mobility $\propto T^{-3/2}$ due to increased scattering $\mu = \mu_0 \left(\frac{300}{T} \right)^{3/2}$
  - Threshold voltage decreases with temperature due to reduced bandgap energy $E_g = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$

I_D vs Temperature

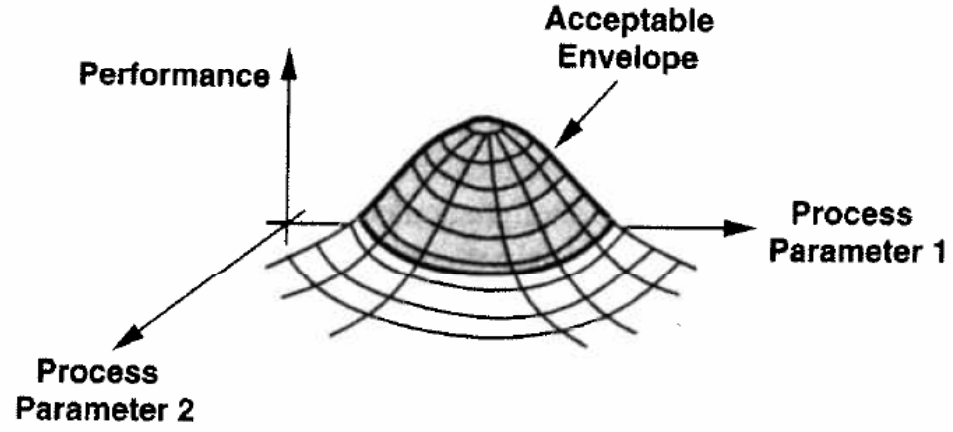


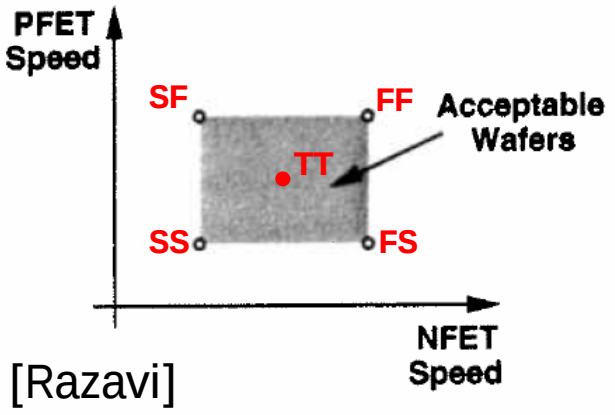
V_T vs Temperature



Process Corners

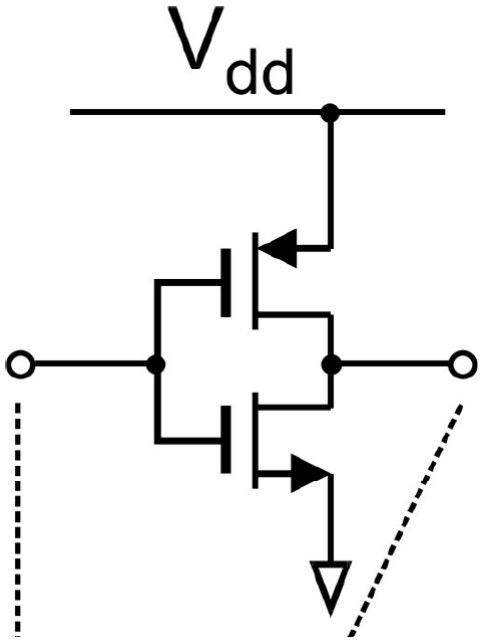
- Substantial process variations can exist from wafer to wafer and lot to lot
- Device characteristics are guaranteed to lie in a performance envelope
- To guarantee circuit yield, designers simulate over the "corners" of this envelope
- Example: Slow Corner
  - Thicker oxide (high V_T, low C_{ox}), low μ, high $R_{\square}$

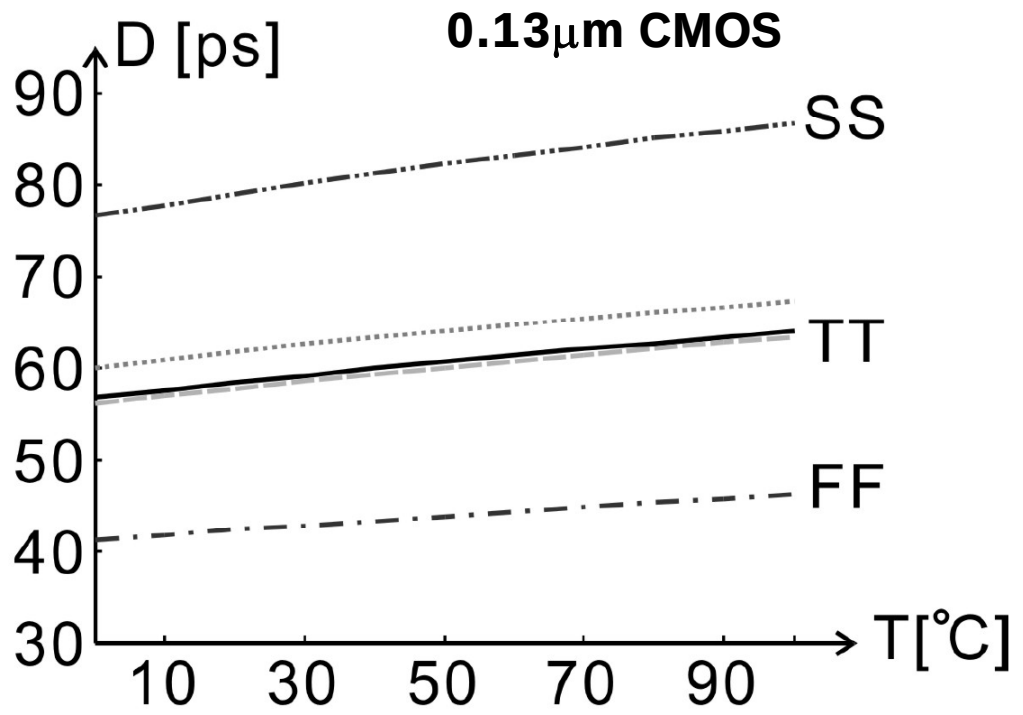




[Razavi]

Inverter Delay Variation with Process & Temperature





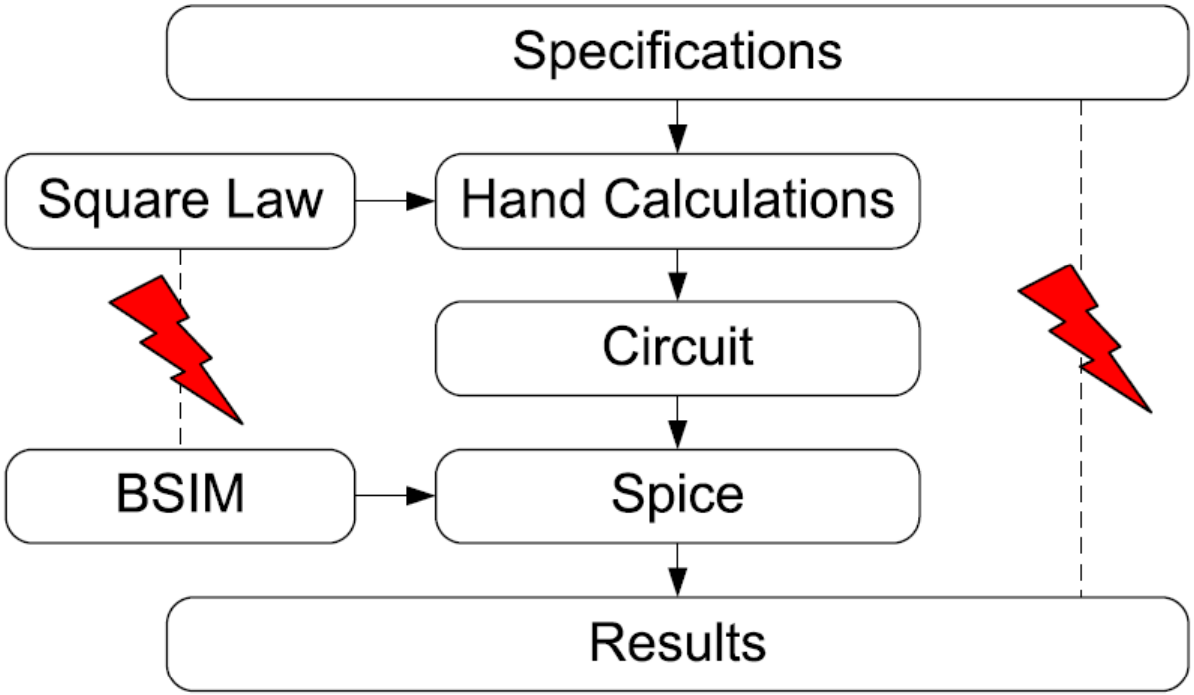
[Woo ISSCC 2009]

- CMOS inverter delay varies close to ±40% over process and temperature

How to Design with Modern Sub-Micron (Nanometer) Transistors?

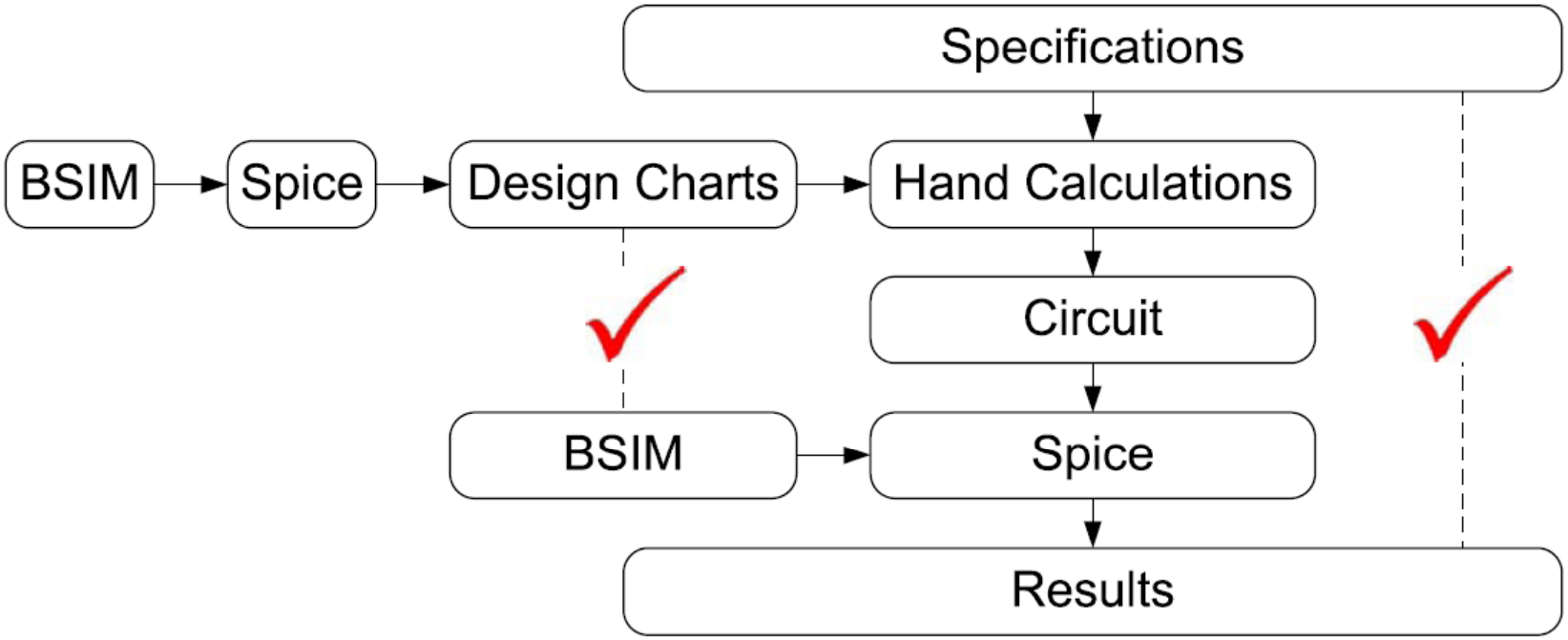
- Hand calculations with square-law model can deviate significantly from actual device performance
  - However, advanced model equations are too tedious for design
- Tempts designers to dive straight to simulation with little understanding on circuit performance trade-offs
  - “Spice Monkey” approach
- How can we accurately design when hand analysis models are way off?
- Employ a design methodology which leverages characterization data from BSIM simulations

The Problem



[Murmann]

The Solution



[Murmann]

Device Figures of Merit

Square-Law

- Transconductance efficiency
  - Want maximum g_m for minimum current

$$\boxed{\frac{g_m}{I_D}} = \frac{2}{V_{OV}}$$

$$V_{OV} = V_{GS} - V_T$$

- Transit frequency, f_T
  - Want maximum g_m for minimum C_{gg}
  - C_{gg} = total gate cap = C_{gs} + C_{gd} +C_{gb}

$$\boxed{\omega_T = \frac{g_m}{C_{gg}}} \cong \frac{3}{2}\frac{\mu V_{OV}}{L^2}$$

assuming $C_{gg} = C_{gs}$ **only**

- Intrinsic gain
  - Want maximum $g_m/g_{ds}=g_m r_o$

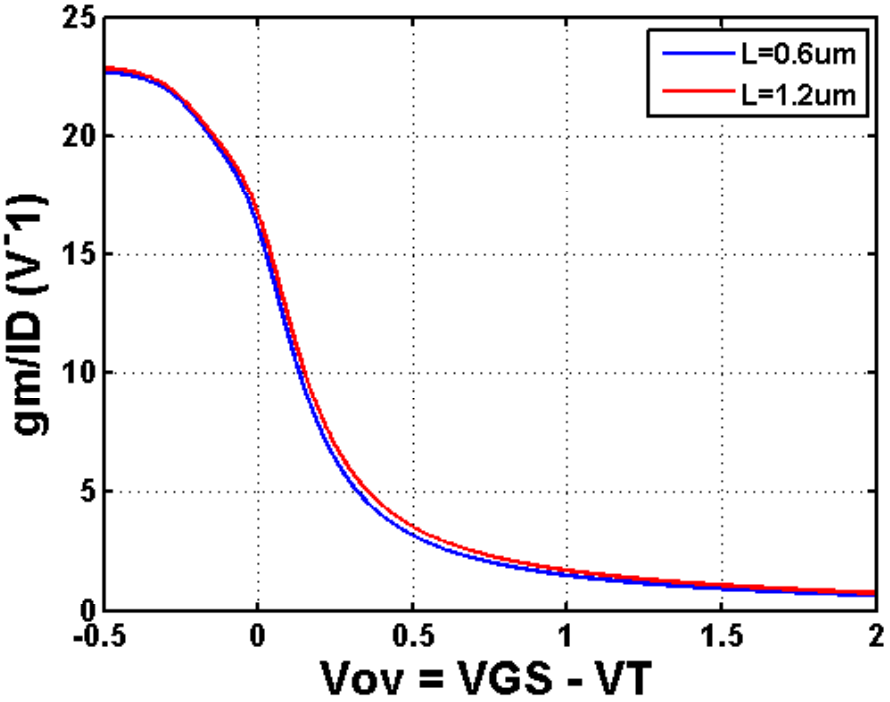
$$\boxed{\frac{g_m}{g_{ds}}} \cong \frac{2}{\lambda V_{OV}}$$

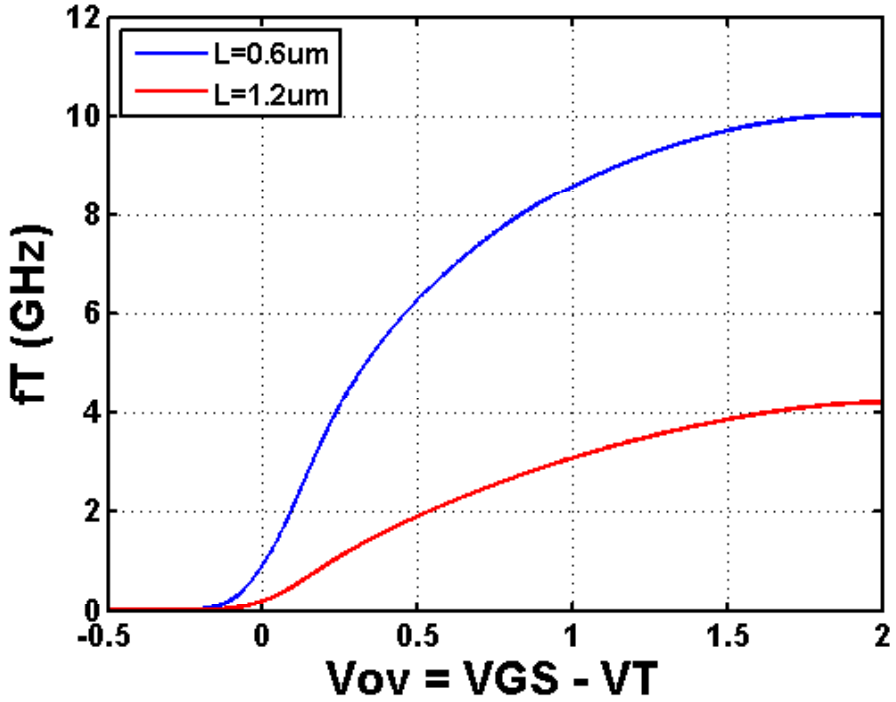
Technology Characterization for Design

- Generate data for the following over a reasonable range of g_m/I_D and channel lengths
  - Transit frequency (f_T)
  - Intrinsic gain (g_m/g_{ds})
  - Current density (I_D/W)
- Also useful is extrinsic capacitor ratios
  - C_{gd}/C_{gg} and C_{dd}/C_{gg}
- Parameters are (to first order) independent of transistor width, which enables “normalized design”
- Do design hand calculations using the generated technology data
- Still need to understand how the circuit operates for an efficient design!!!

Our 0.6um Technology Simulation Data

NMOS W=2.4um





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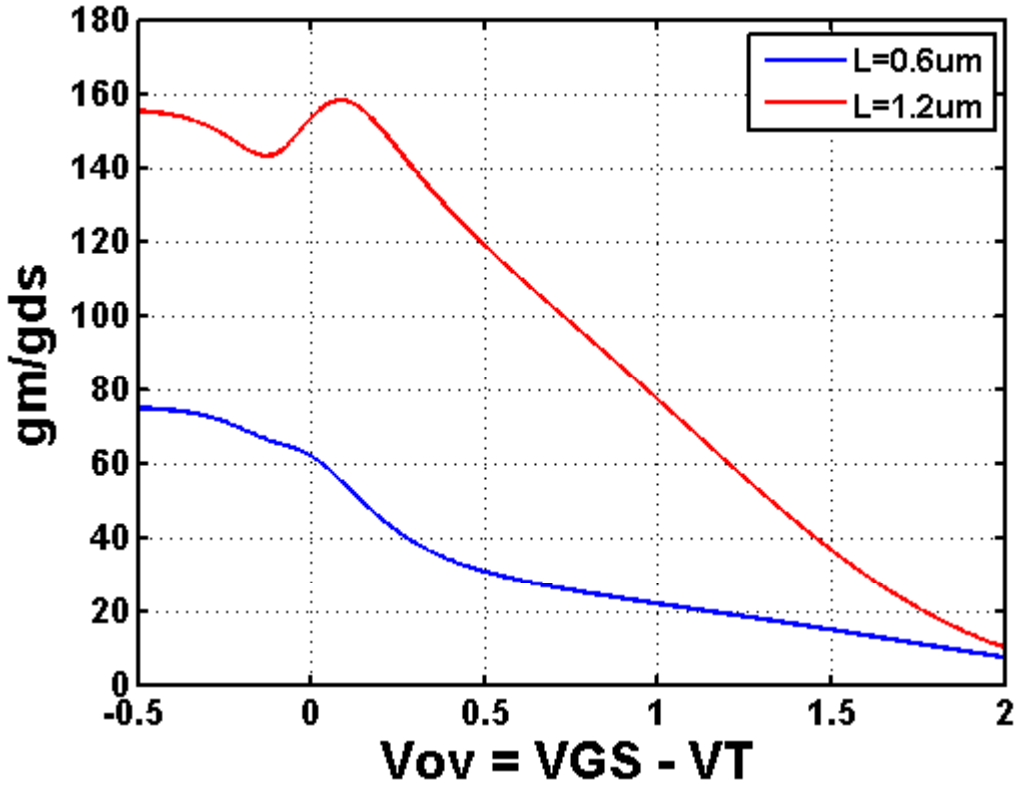

Next Time

- Layout Techniques