ECEN474: (Analog) VLSI Circuit Design
Fall 2011

Lecture 3: MOS Transistor Modeling

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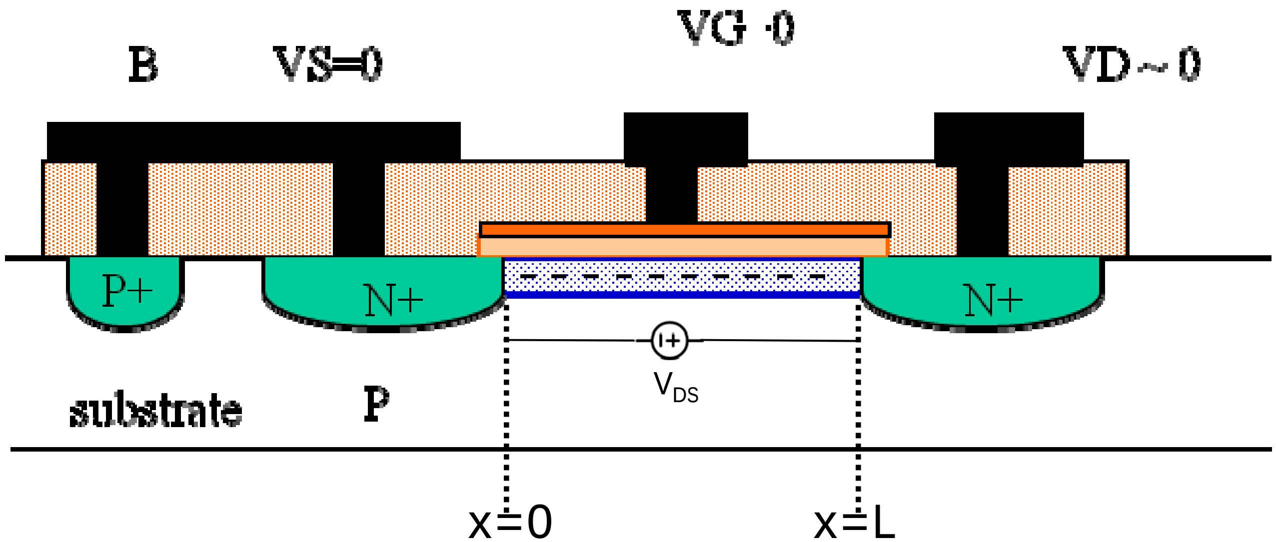
Announcements

- No Lab this week
  - Lab 1 next week
- Current Reading
- Razavi’s CMOS book chapter 2

Agenda

- MOS Transistor Modeling
  - Large-Signal “DC” Model
  - Small-Signal “AC” Model
  - MOS Capacitors

Triode Region



[Silva]

$V(0)=0$ $V(x)=V_{DS}\frac{x}{L}$ $V(L)=V_{DS}$

$$V_{GC}(x)=V_{GS}-V(x)=V_{GS}-V_{DS}\frac{x}{L}$$

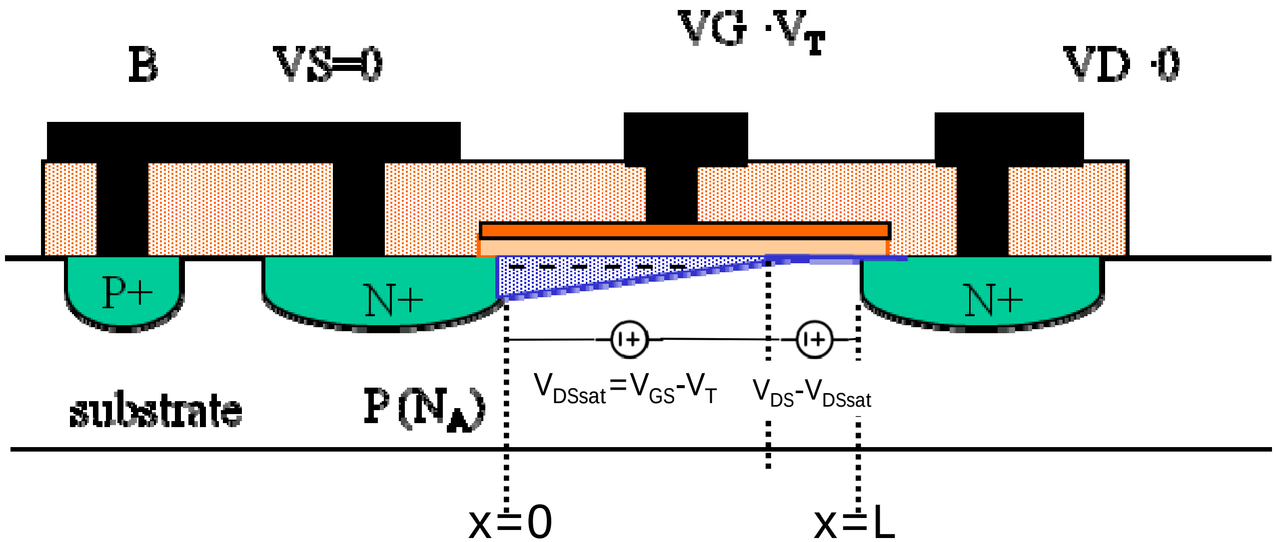
- Channel depth and transistor current is a function of the overdrive voltage, V_{GS}-V_T, and V_{DS}
- Because V_{DS} is small, V_{GC} is roughly constant across channel length and channel depth is roughly uniform

$$\boxed{I_{DS}=\frac{W}{L}\mu_n C_{OX}\left(V_{GS}-V_{Tn}-0.5V_{DS}\right)V_{DS}}$$

For small V_{DS}

$$\boxed{R_{DS}\approx\frac{1}{\frac{W}{L}\mu C_{ox}\left(V_{GS}-V_{Tn}\right)}}$$

Saturation Region



[Silva]

$V(0)=0 \quad V(x)=V_{DS}\frac{x}{L} \quad V(L)=V_{DS}$

$$V_{GC}(x)=V_{GS}-V(x)=V_{GS}-V_{DS}\frac{x}{L}$$

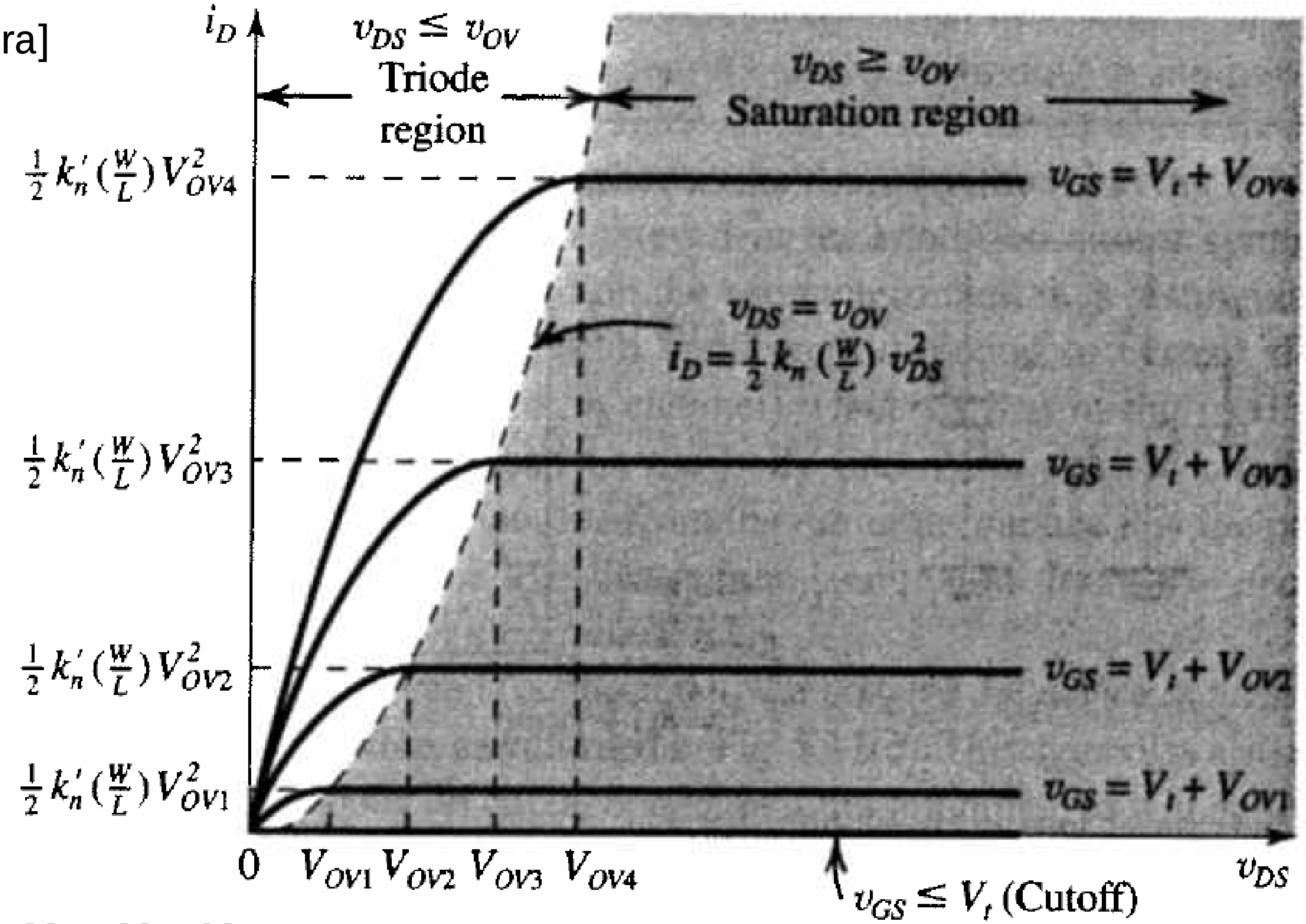
- Channel “pinches-off” when $V_{DS}=V_{GS}-V_T$ and the current saturates
- After channel charge goes to 0, the high lateral field “sweeps” the carriers to the drain and drops the extra V_{DS} voltage

$$\boxed{I_{DS}=\frac{W}{2L}\mu_n C_{OX}\left(V_{GS}-V_{Tn}\right)^2}$$

$$\boxed{V_{DSsat}=V_{GS}-V_T}$$

MOS "Large-Signal" Output Characteristic

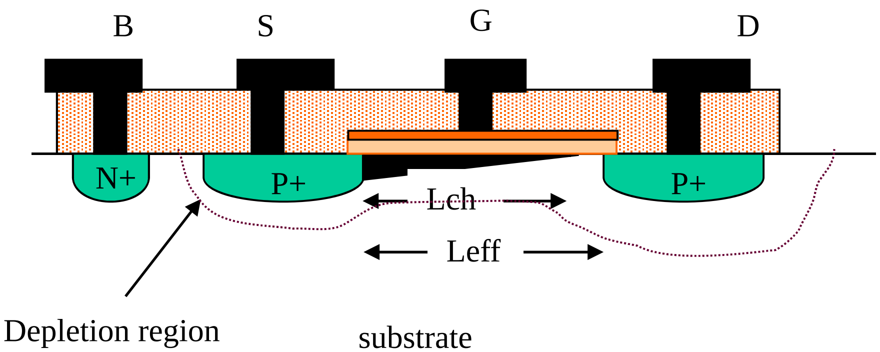
[Sedra]



Note: V_{ov}=V_{GS}-V_T

OUTPUT RESISTANCE (SATURATION REGION)

SATURATION REGION



•Real channel length

$$L_{ch} = L_{drawn} - 2L_D - \Delta L$$

L_D is side diffusion

ΔL is due to channel modulation

•Drain current becomes

$$i_D = \frac{\mu C_{OX}}{2} \frac{W}{L_{ch}} [V_{GS} - V_T]^2$$

$$i_D = \frac{\mu C_{OX}}{2} \frac{W}{L_{eff} - \Delta L} [V_{GS} - V_T]^2$$

This effect is represented in SPICE by using λ

$$error \approx \frac{\Delta L}{L_{eff}}, \qquad \Delta L \propto V_{DS}$$

$$i_D \cong \frac{\mu C_{OX}}{2} \frac{W}{L_{eff}} [V_{GS} - V_T]^2 [1 + \lambda V_{DS}]$$

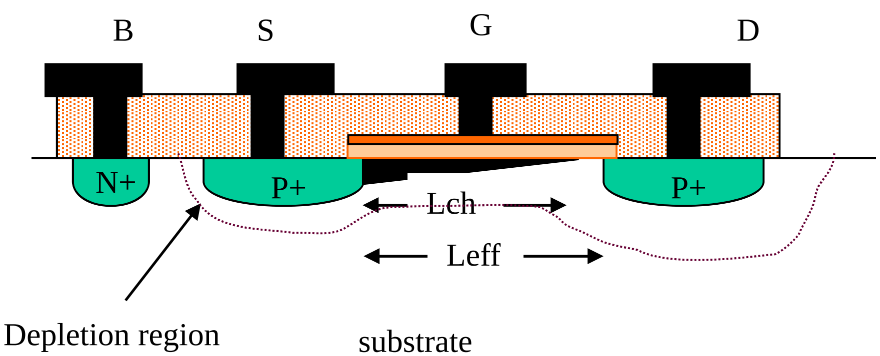
$$\frac{\Delta L}{L_{eff}} = \lambda V_{DS}$$

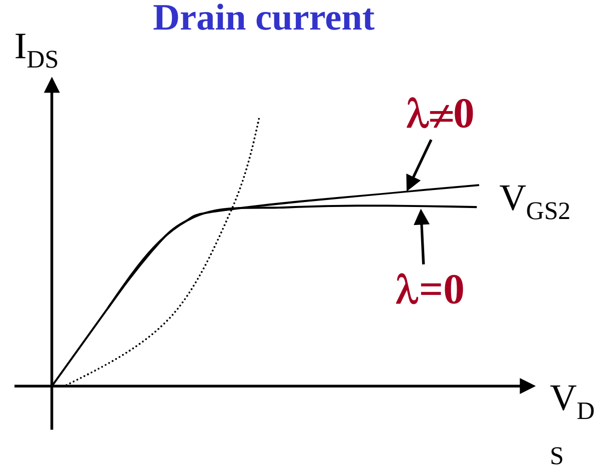
Ideally λ→0

Inversely proportional to L!!!!!

OUTPUT RESISTANCE (SATURATION REGION)

Channel Length Modulation





Channel length modulation is a second (unreliable) order effect!

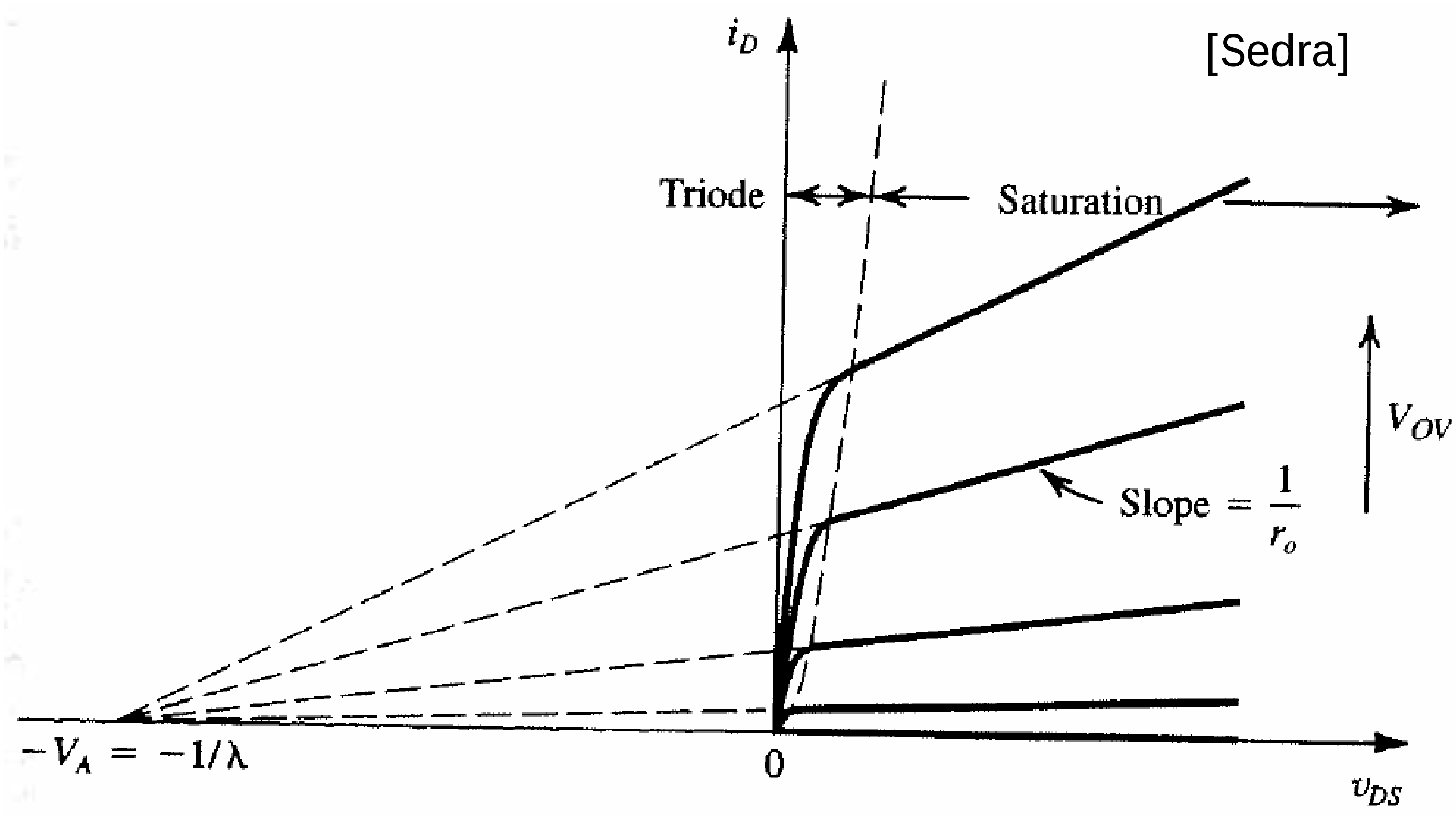
(Badly) Represented in SPICE by using λ or a more complex model.

Simulated and experimental results might be off by more than 100%

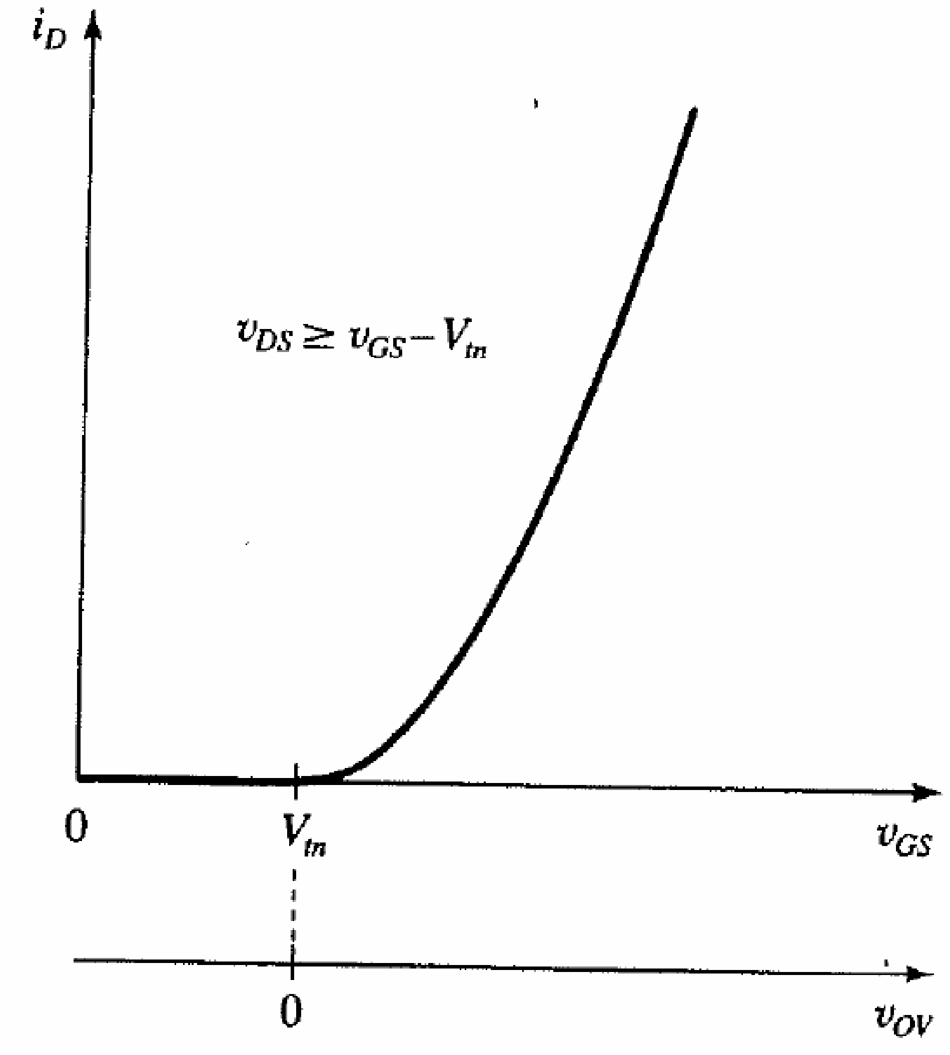
$$i_D \cong \frac{\mu C_{OX}}{2} \frac{W}{L_{eff}} \left[V_{GS} - V_T\right]^2 \left[1 + \lambda V_{DS}\right]$$

Measure this parameter!

MOS “Large-Signal” Output Characteristic with Finite Output Resistance

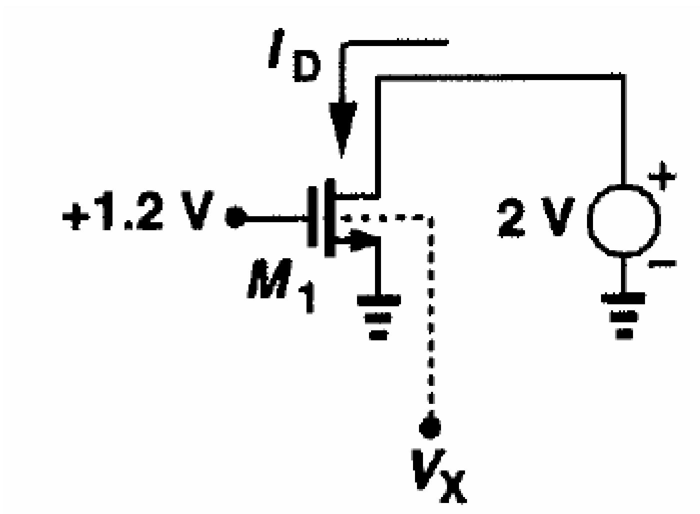


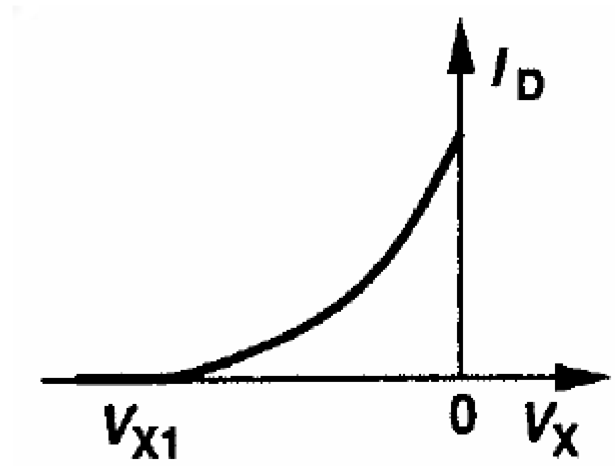
MOS "Large-Signal" Transfer Characteristic



[Sedra]

Impact of Bulk Voltage



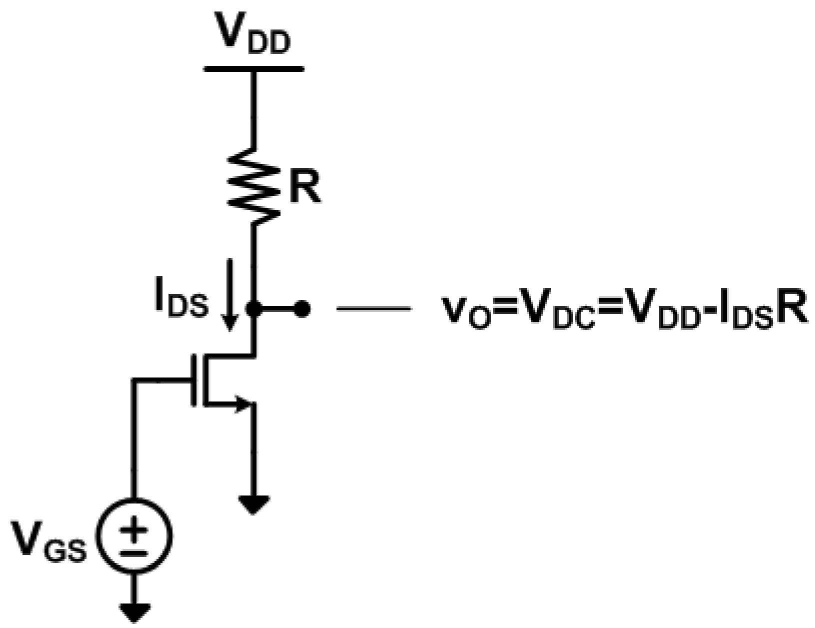


[Razavi]

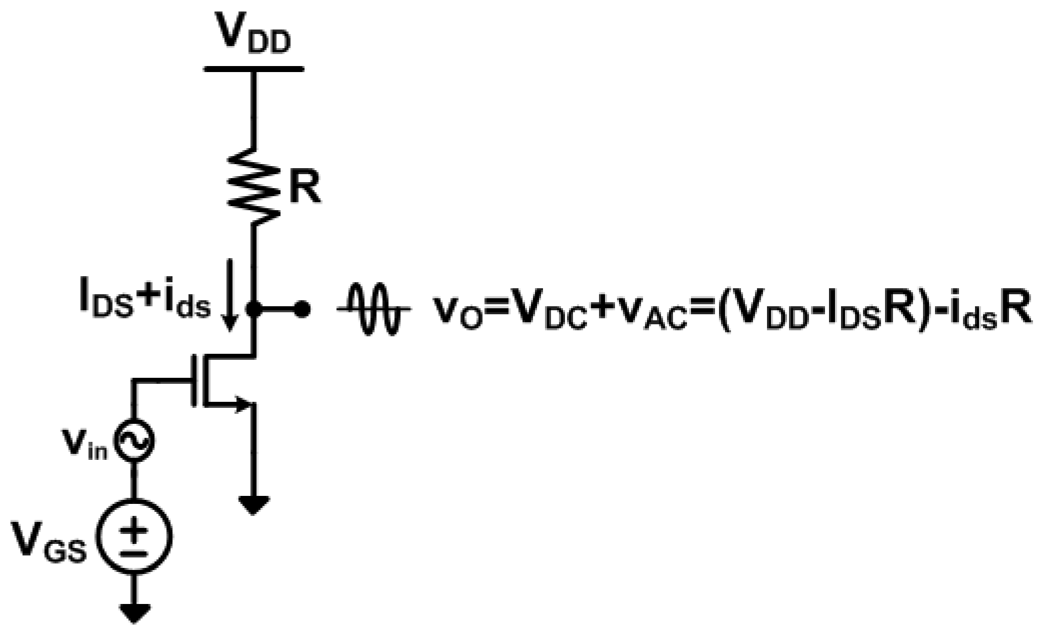
$$V_T = V_{T0} + \gamma\left[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right] \Rightarrow V_{T0}\Big|_{V_{SB}=0}$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_{Bulk}}}{C_{OX}} \longrightarrow$$ Body Effect Coefficient

Large-Signal “DC” Response



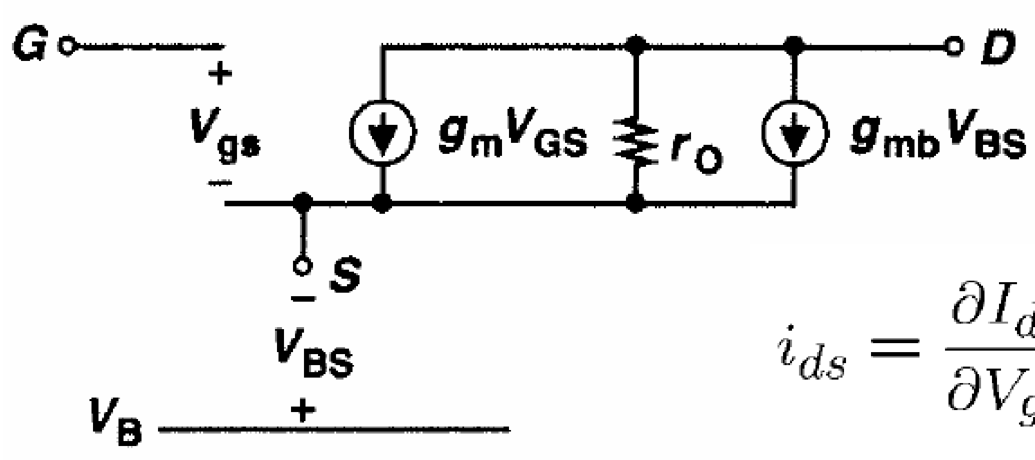
Large-Signal “DC” + Small-Signal “AC” Response



- For small-signal analysis, we “linearize” the response about the DC operating point
- If the signal is small enough, linearity holds and the complete response is the summation of the large-signal “DC” response and the small-signal “AC” response

Low-Frequency Small-Signal Model

[Razavi]



$$i_{ds} = \frac{\partial I_{ds}}{\partial V_{gs}} v_{gs} + \frac{\partial I_{ds}}{\partial V_{bs}} v_{bs} + \frac{\partial I_{ds}}{\partial V_{ds}} v_{ds}$$

$$i_{ds} = g_m V_{gs} + g_{mb} V_{bs} + g_{ds} V_{ds}$$

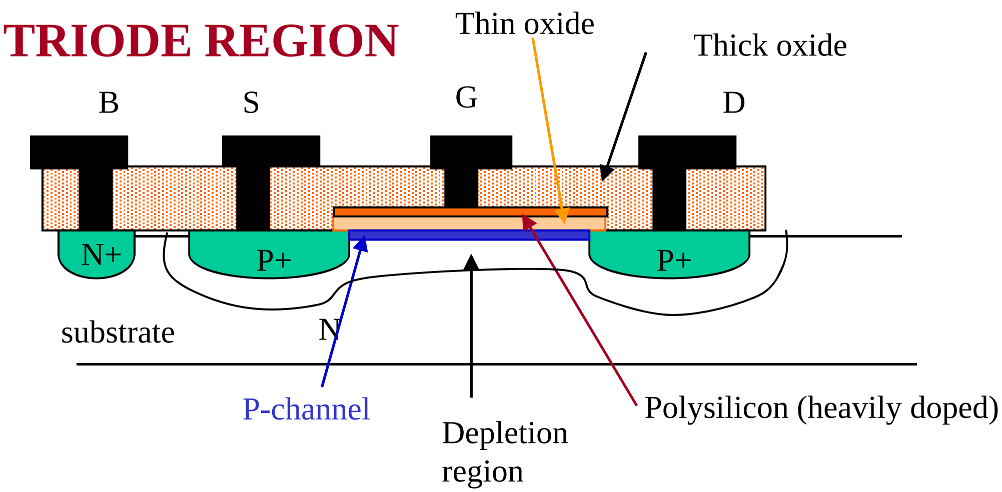
$$g_m = \left.\frac{\partial i_D}{\partial v_{gs}}\right|_Q \approx \mu C_{OX} \frac{W}{L_{eff}} \left.(V_{GS} - V_T)\right|_Q$$ → MOS transconductance

$$1/ro = g_0 = \left.\frac{\partial i_D}{\partial v_{ds}}\right|_Q \approx \left.\left(\frac{\mu C_{OX}}{2}\right)\left(\frac{W}{L_{eff}}(V_{GS} - V_T)^2\right)\right|_Q \lambda \cong \lambda I_D$$ → Channel length modulation effect

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{bs}}\right|_Q \approx \mu C_{OX} \left.\frac{W}{L_{eff}}[V_{GS} - V_T]\right|_Q * \left(-\left.\frac{\partial V_T}{\partial v_{bs}}\right|_Q\right) \cong \frac{\gamma g_m}{2\sqrt{2\phi_F + V_{SB}}}$$ → Body effect

MOS Transistor: CAPACITORS

TRIODE REGION



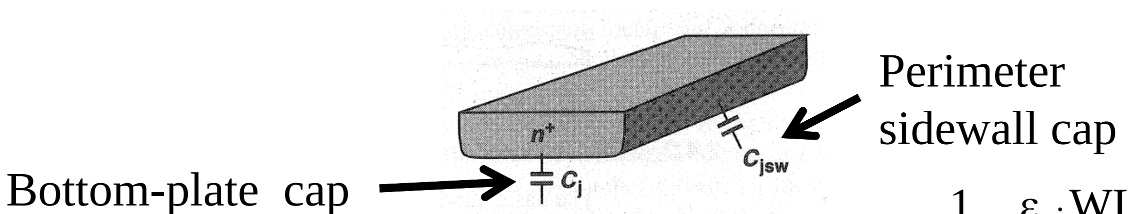
•GATE-CHANNEL CAPACITANCE

$$C_{G-CH} = WLC_{OX}$$

•Effective channel length (lateral diffusion)
Leff=L-2LD

$$C_{G-CH} = WL_{eff}C_{OX}$$

•CHANNEL-BULK CPACITANCE



$$C_{Ch-b} = \frac{\varepsilon_{si} WL_{eff}}{t_{si}}$$

•SOURCE-BULK CAPACITANCE

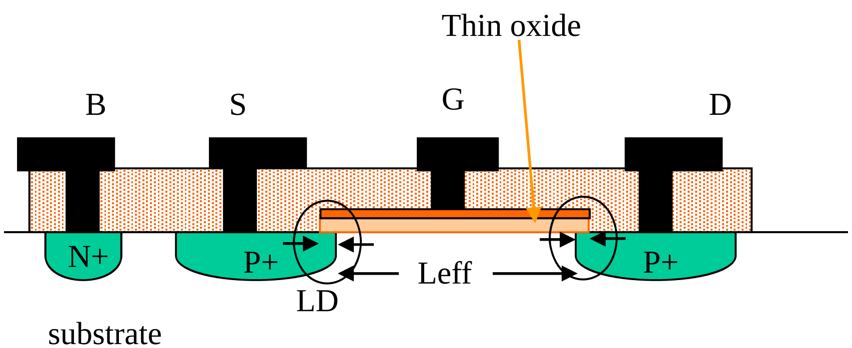
$$C_{s-b} = \frac{1}{2} * \frac{\varepsilon_{si} WL_{eff}}{t_{si}} + C_{bottom-source} + C_{sw-source}$$

•DRAIN-BULK CPACITANCE

$$C_{d-b} = \frac{1}{2} * \frac{\varepsilon_{si} WL_{eff}}{t_{si}} + C_{bottom-drain} + C_{sw-drain}$$

CAPACITANCES (CGS, CGD)

Lateral diffusion effects



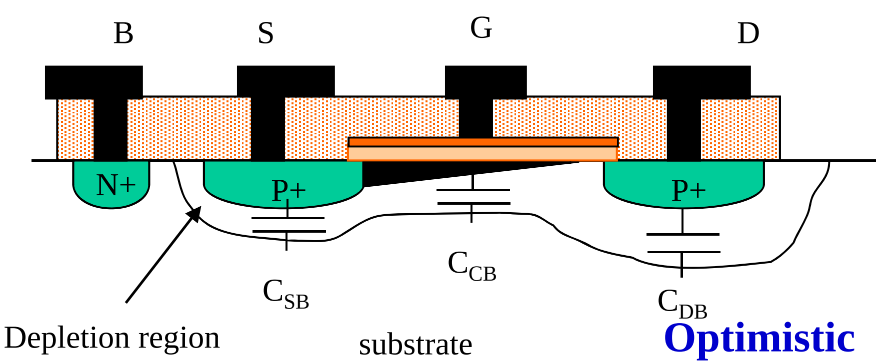
•Under diffusions overlap the transistor terminals and the gate leading to the overlapping capacitances

$$C_{GS-OV} = C_{GD-OV} = WL_D C_{OX}$$

LD is technology dependent (SPICE PARAMETER)

•Effective channel length Leff=L-2LD

SATURATION REGION



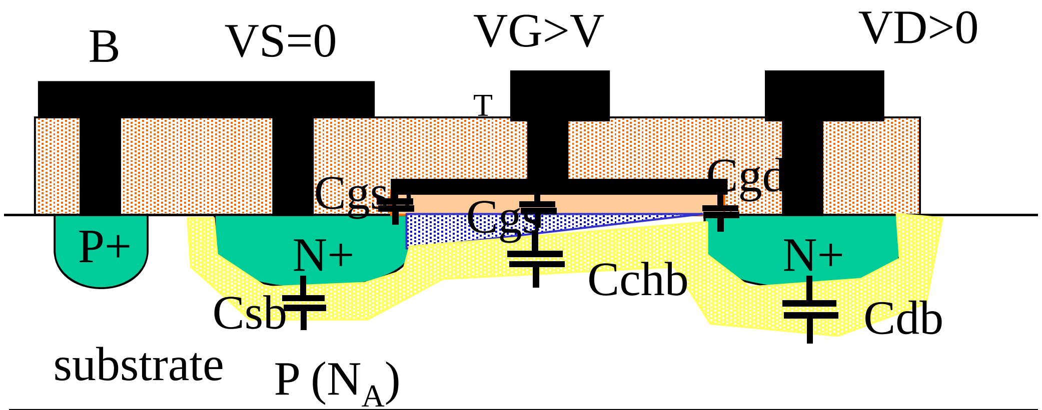
C_{SB} → Source bulk (junction capacitor)

C_{DB} →Source bulk (junction capacitor)

C_{ChB} →Channel-bulk (junction capacitor)

Optimistic $C_{Ch-b}=\frac{2}{3}*\frac{\varepsilon_{si}WL_{eff}}{t_{si}}, \quad t_{si}(V_{ch-b})\sim t_{si}(V_{s-b})$

Transistor Model: Capacitances



$$C_{SB} = Cjb + Cjsw$$

$$C_{DB} = Cjb + Cjsw$$

$$C_{ChB} = Cj * W * L$$

Triode

$$C_{GS} = \frac{\varepsilon_{OX}}{t_{OX}} * \frac{W*L}{2} + \frac{\varepsilon_{OX}}{t_{OX}} * W * L_D$$

$$C_{GD} = C_{GS}$$

$$C_{SB} = Cjs * As + Cjsw * Ps + Cjs * \frac{W*L}{2}$$

$$C_{DB} \cong Cjd * Ad + Cjsw * Pd + Cjd * \frac{W*L}{2}$$

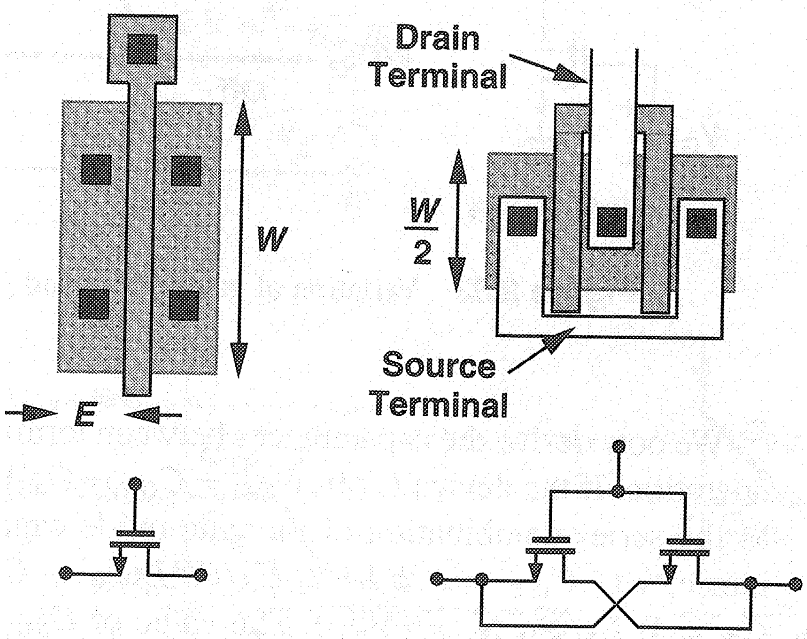
Saturation

$$C_{GS} = \frac{2}{3} * \frac{\varepsilon_{OX}}{t_{OX}} * W * L + \frac{\varepsilon_{OX}}{t_{OX}} * W * L_D$$

$$C_{GD} = \frac{\varepsilon_{OX}}{t_{OX}} * W * L_D$$

$$C_{SB} = Cjs * As + Cjsw * Ps + \frac{2}{3} * Cjs * W * L$$

$$C_{DB} \cong Cjd * Ad + Cjsw * Pd$$



(a) (b)

Figure 2.32

Solution

For the transistor in Fig. 2.32(a), we have

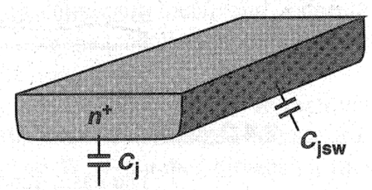
$$C_{DB} = C_{SB} = WEC_j + 2(W + E)C_{jsw},$$

whereas for that in Fig. 2.32(b),

$$C_{DB} = \frac{W}{2}EC_j + 2\left(\frac{W}{2} + E\right)C_{jsw}$$

$$C_{SB} = 2\left[\frac{W}{2}EC_j + 2\left(\frac{W}{2} + E\right)C_{jsw}\right]$$

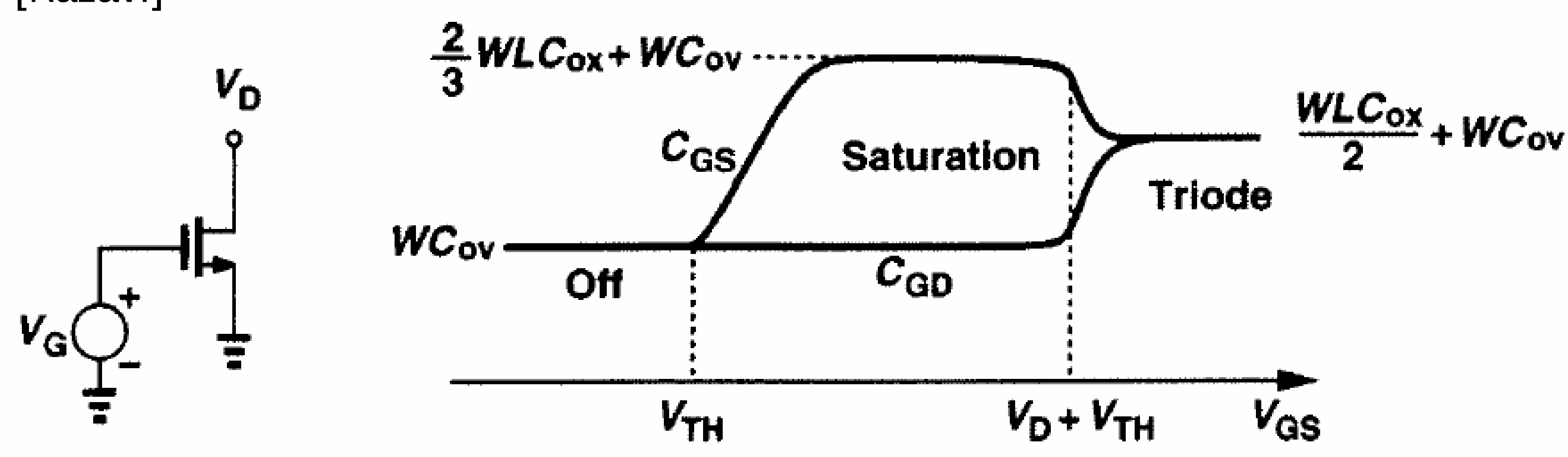
$$= WEC_j + 2(W + 2E)C_{jsw}.$$



MOS Gate Capacitors Response

Note: $C_{ov}=L_D C_{ox}$

[Razavi]

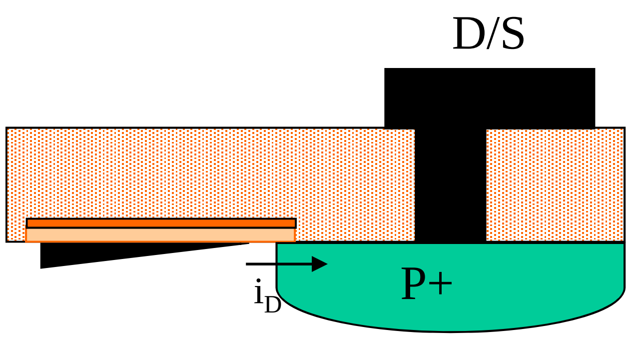


Capacitances in 0.25 um CMOS Process

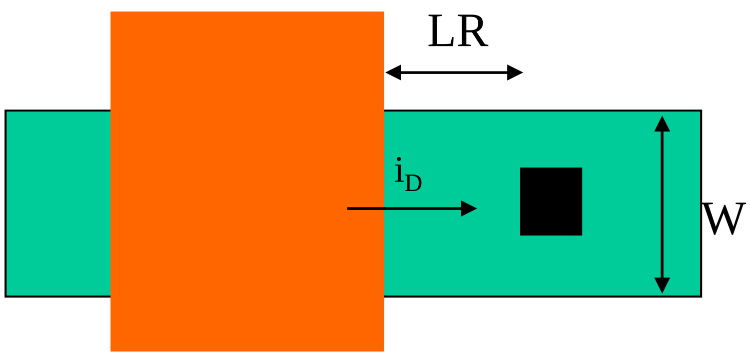
	Cox(fF/um²)	*Cov(fF/um²)*	*Cj(fF/um²)*	*Cjsw(fF/um²)*
NMOS	6	0.31	2	0.28
PMOS	6	0.27	1.9	0.22

Other resistors: Source/Drain

Drain/Source Resistance



Top view



•**Drain/Source Resistance**

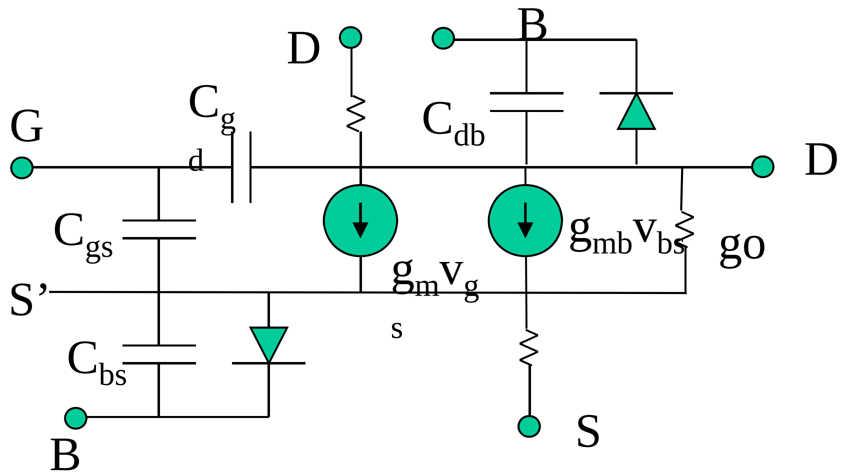
In addition to the contact resistance , the diffusion resistance has to be considered.

$$R_{series} = \frac{L_R}{W}\left(R_{[]}\right)$$

$$R_{series} = \left(\frac{L_R}{W}\right)\left(\frac{\delta}{t}\right)$$

•**In SPICE, $R_{[]}$ is defined as RSH**

Small Signal Model (Saturation region)



Small signal model (saturation region)

$$i_D = \frac{\mu C_{OX}}{2}\frac{W}{L_{eff}}\left[V_{GS}-V_T\right]^2\left[1+\lambda V_{DS}\right]$$

$$V_T = V_{T0} + \gamma\left[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right]$$

$$i_D = \frac{\mu C_{OX}}{2}\frac{W}{L_{eff}}\left[V_{GS}-V_T\right]^2\left[1+\lambda V_{DS}\right]\Big|_Q + \frac{\partial i_D}{\partial v_{gs}}\Big|_Q v_{gs} + \frac{\partial i_D}{\partial v_{ds}}\Big|_Q v_{ds} + \frac{\partial i_D}{\partial v_{bs}}\Big|_Q v_{bs} + \ldots.$$

$$\boxed{i_D \cong I_D + g_m v_{gs} + g_0 v_{ds} + g_{mb} v_{bs}}$$

$$g_m = \frac{\partial i_D}{\partial v_{gs}}\Big|_Q \approx \mu C_{OX}\frac{W}{L_{eff}}\left(V_{GS}-V_T\right)\Big|_Q$$

$$g_0 = \frac{\partial i_D}{\partial v_{ds}}\Big|_Q \approx \left(\frac{\mu C_{OX}}{2}\right)\left(\frac{W}{L_{eff}}\left(V_{GS}-V_T\right)^2\right)\Big|_Q \lambda$$

$$g_{mb} = \frac{\partial i_D}{\partial v_{bs}}\Big|_Q \approx \mu C_{OX}\frac{W}{L_{eff}}\left[V_{GS}-V_T\right]\Big|_Q * \left(-\frac{\partial V_T}{\partial v_{bs}}\Big|_Q\right) \cong \frac{\gamma g_m}{2\sqrt{2\phi_F + V_{SB}}}$$