ECEN474: (Analog) VLSI Circuit Design
Fall 2011

Lecture 2: MOS Transistor Modeling

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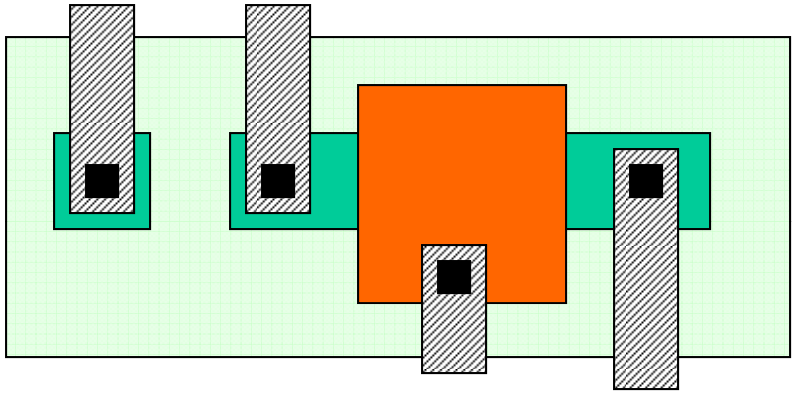
Announcements

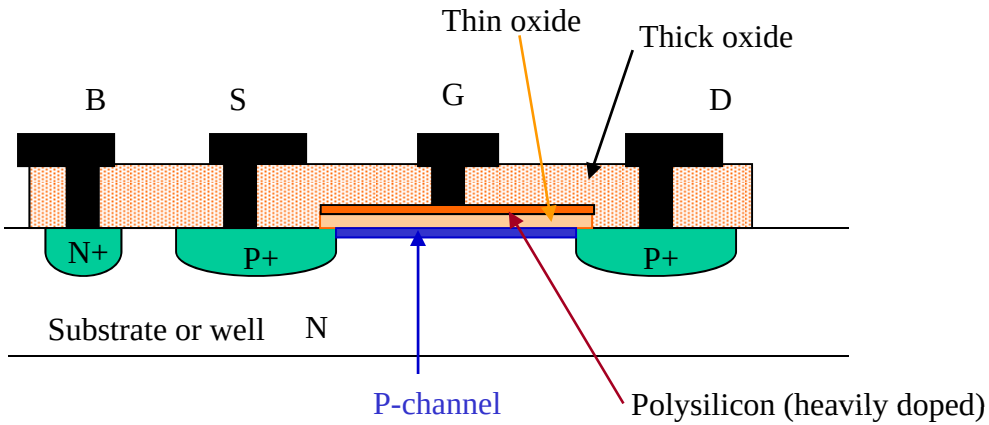
- No Lab this week
  - Lab 1 next week
- Current Reading
  - Razavi's CMOS book chapter 2

Agenda

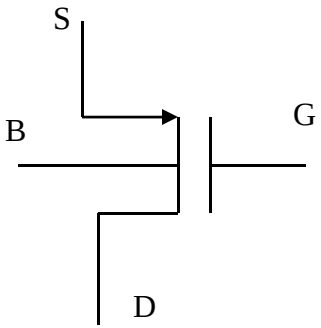
- MOS Transistor Modeling
  - DC I-V Equations
  - Threshold Voltage, V_T

MOS Transistor





P-type transistor



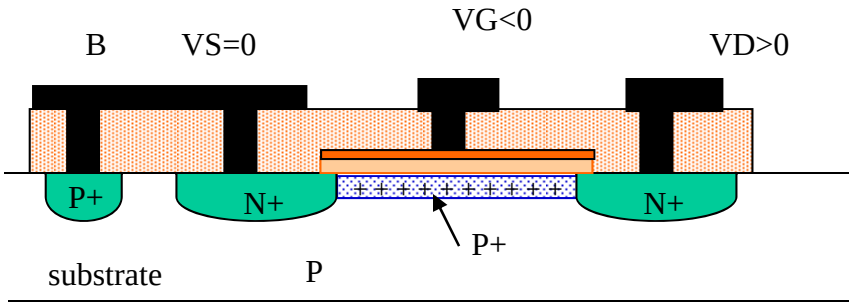
BASIC IDEA:

SOURCE-DRAIN CURRENT IS CONTROLLED BY THE SOURCE-GATE VOLTAGE.

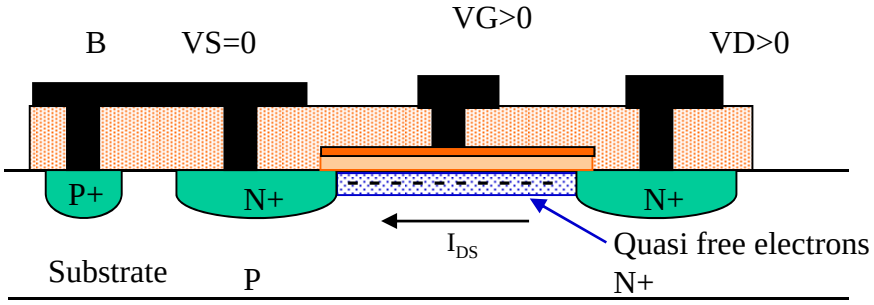
The system is “isolated” if the diodes are biased in reverse region by using the Bulk terminal.

MOS Transistor

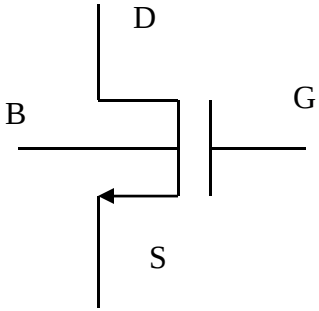
Accumulation: Two diodes back to back
D-S current is zero



Inversion: Channel is connecting D and S
D-S current is possible



N-type transistor



Under this condition, there are 3 possible applications:

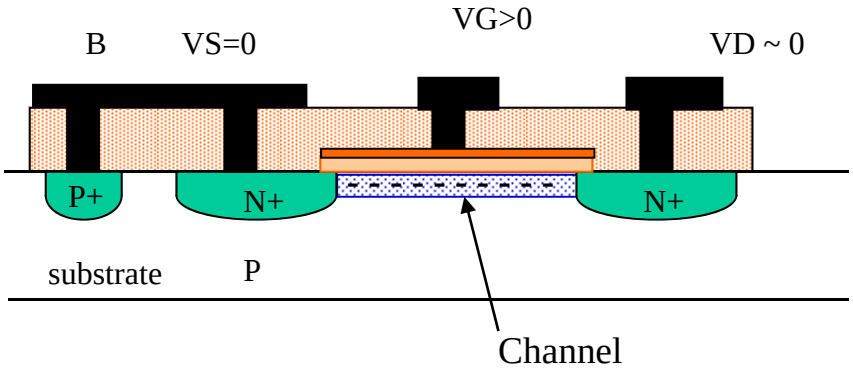
Subthreshold (extremely low-voltage low-power applications)

Linear region (voltage controlled resistor, linear OTA's, multipliers, switches)

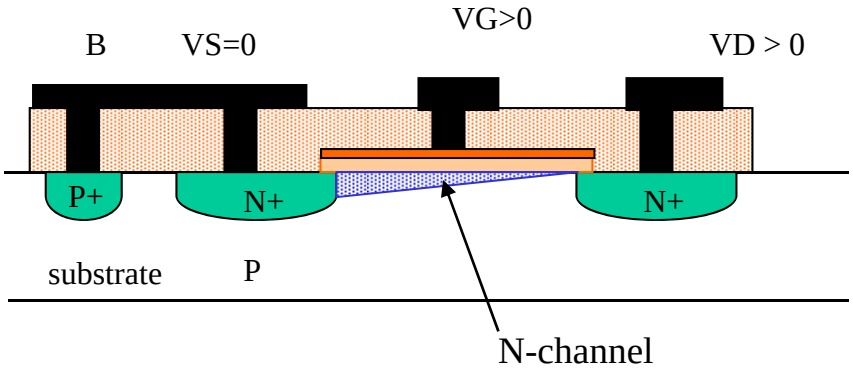
Saturation region (Amplifiers)

MOS Transistor

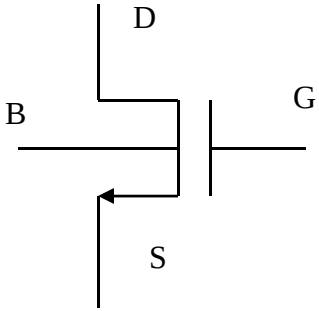
Triode Region (D-S channel is complete)



Saturation Region (D-S channel is incomplete)



N-type transistor



In this condition, there are 3 possible applications:

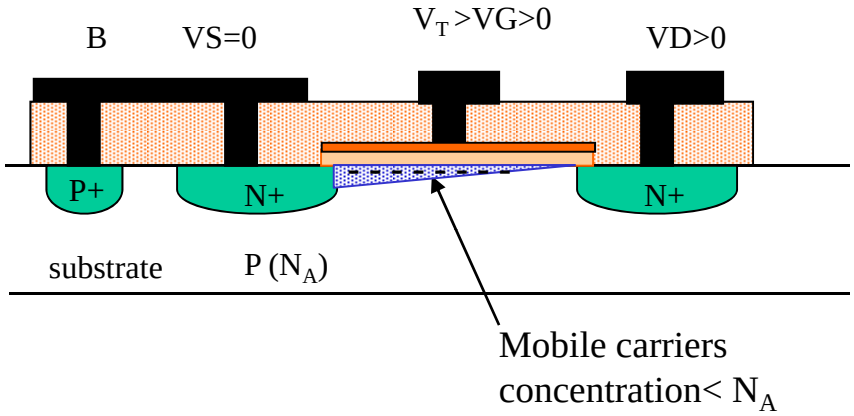
Subthreshold (extremely low-voltage low-power applications)

Linear region (voltage controlled resistor, linear OTA's, multipliers)

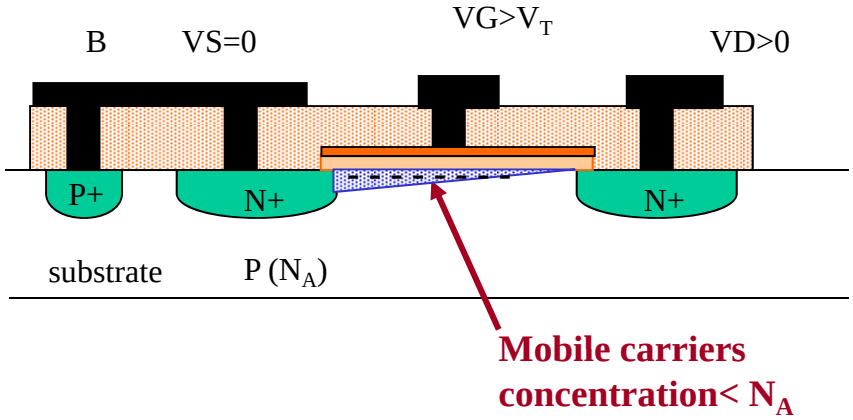
Saturation region (Amplifiers)

MOS Transistor

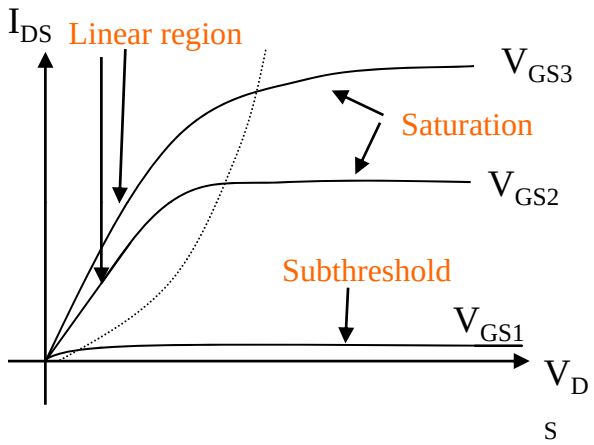
Subthreshold (weak inversion)



Saturation (Strong inversion)



N-type transistor

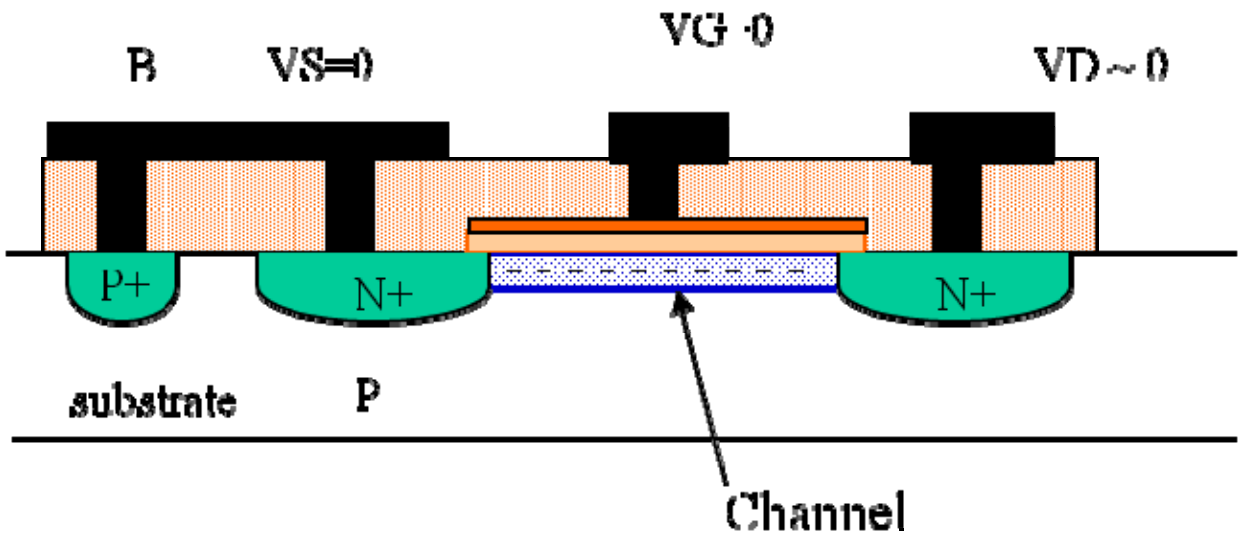


Subthreshold (extremely low-voltage low-power applications)

Linear region (voltage controlled resistor, linear OTA's, multipliers)

Saturation region (Amplifiers)

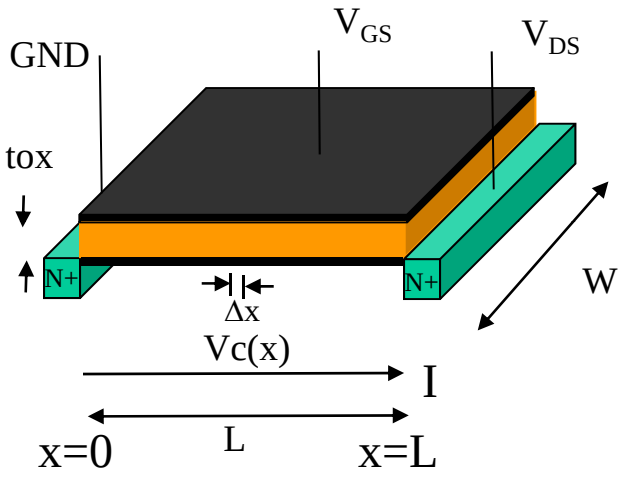
V_T Definition



[Silva]

- The threshold voltage, V_T, is the voltage at which an “inversion layer” is formed
  - For an NMOS this is when the concentration of electrons equals the concentration of holes in the p^- substrate

MOS Equations in Linear Region



$$I = Q_d \upsilon$$ Source-Drain Current

$$Q_d(x) = WC_{OX}(V_{GC} - V_T)$$ Incremental Charge Density

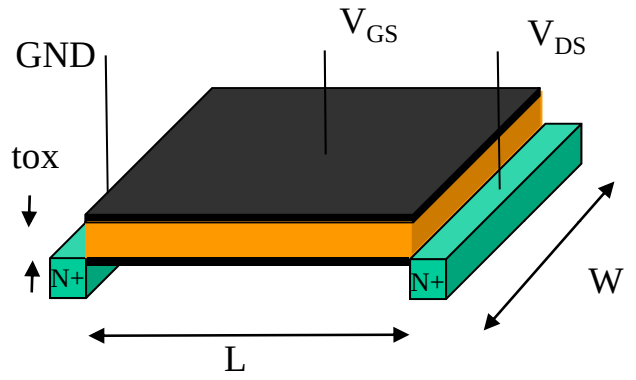
$$V_{GC} - V_T = V_{GS} - V_{CS}(x) - V_T$$ Gate-channel Voltage

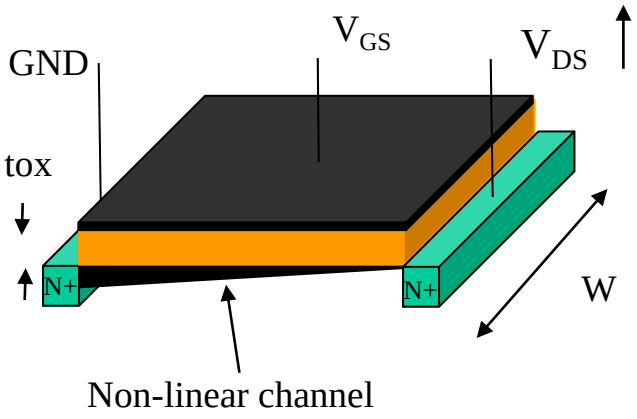
$$I_D = -WC_{OX}(V_{GS} - V_{CS}(x) - V_T)\upsilon$$ Drain-Source Current

$$I_D = WC_{OX}(V_{GS} - V_{CS}(x) - V_T)\mu_n \frac{dV(x)}{dx}$$

$$\int_{x=0}^{L} I_D dx = \int_{V=V_S}^{V_D} WC_{OX}(V_{GS} - V_{CS}(x) - V_T)\mu_n dV$$

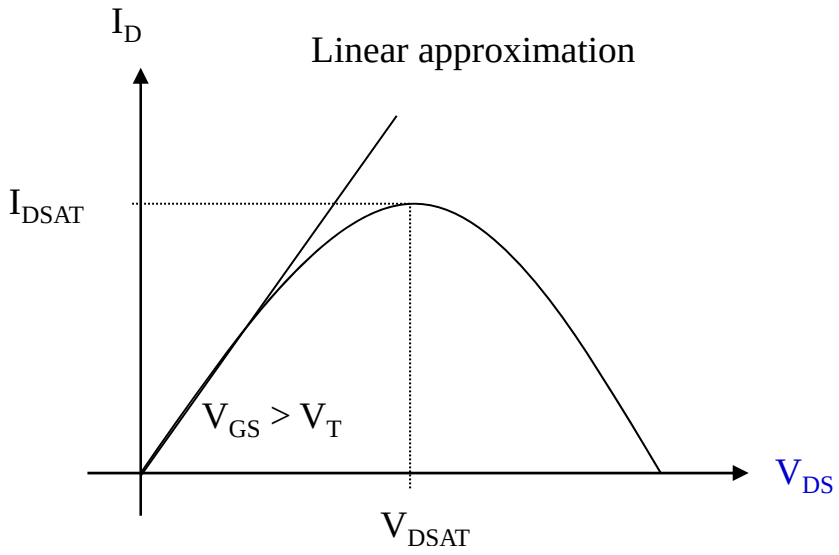
MOS Equations in **Linear Region**



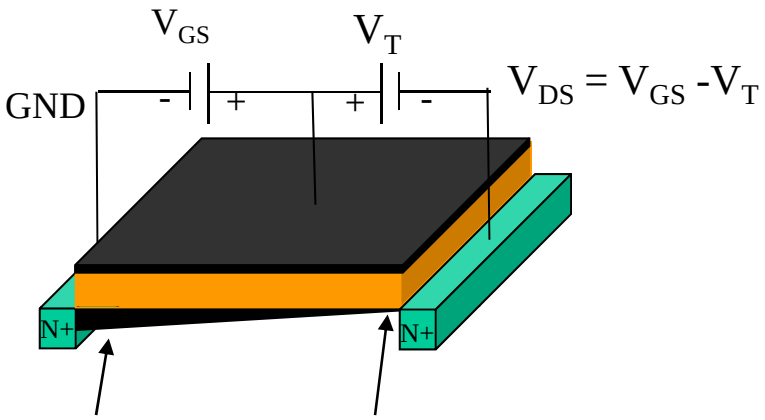


Drain current: Expression used in SPICE level 1

$$I_D = \frac{W}{L}\mu_n C_{OX}\left(V_{GS} - V_T - 0.5V_{DS}\right)V_{DS}$$



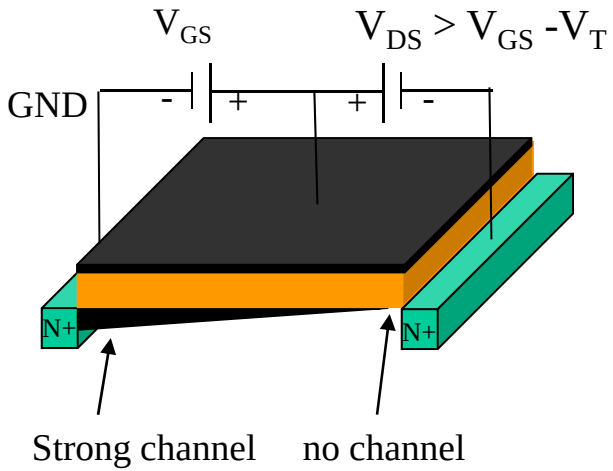
MOS Equations in **Saturation and Linear Region**



Under these conditions → current is highest

$$I_D = \frac{W}{2L}\mu_n C_{OX}\left(V_{GS} - V_T\right)^2$$

SATURATION REGION ($V_{DS} > V_{GS} - V_T$)



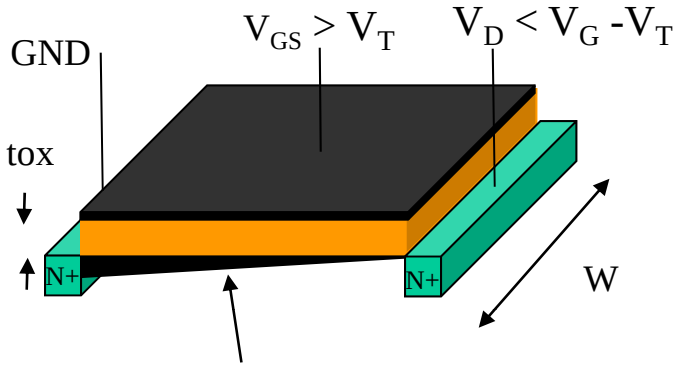
Carriers are attracted to the drain, and swept in the region where channel is incomplete (why??)

Current is till given by $I_D = \frac{W}{2L}\mu_n C_{OX}\left(V_{GS} - V_T\right)^2$

or

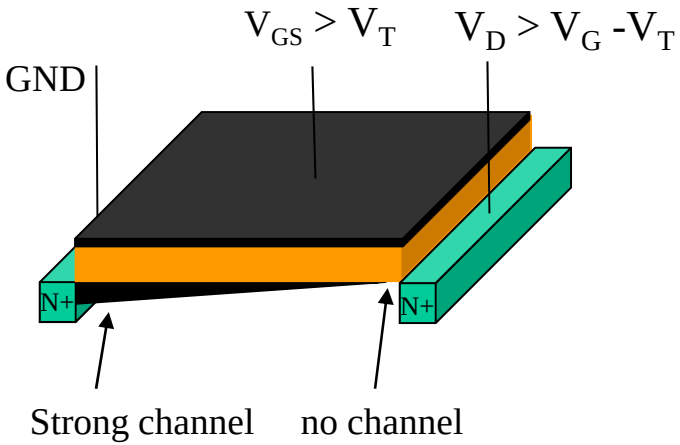
SPICE level 1 $I_{DSAT} = \frac{W}{2L}\mu_n C_{OX}\left(V_{DSAT}\right)^2$

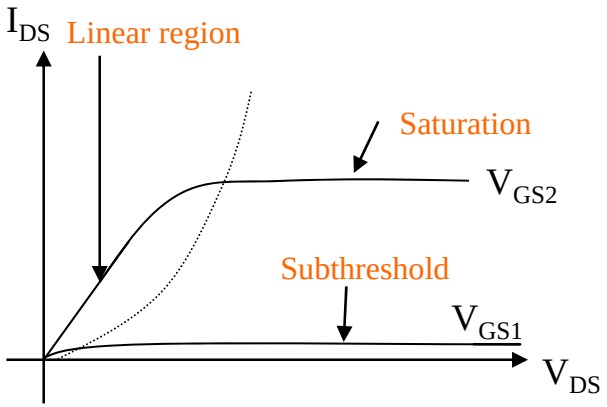
MOS Equations in **Saturation and Linear Region: $V_{GS}>V_T$**



Linear region: $$I_D=\frac{W}{L}\mu_n C_{OX}\left(V_{GS}-V_T-0.5V_{DS}\right)V_{DS}$$

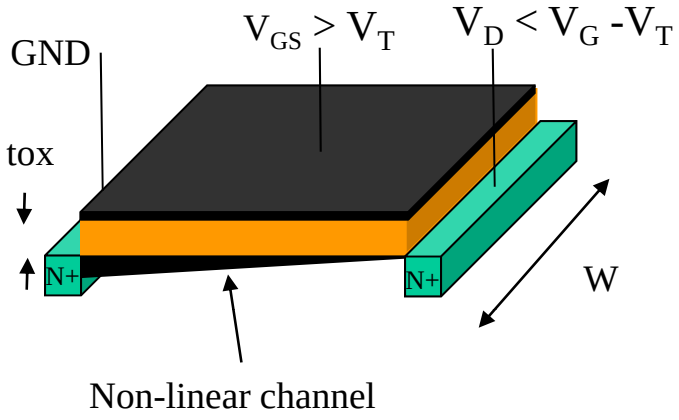
Saturation region: $$I_D=\frac{W}{2L}\mu_n C_{OX}\left(V_{GS}-V_T\right)^2$$





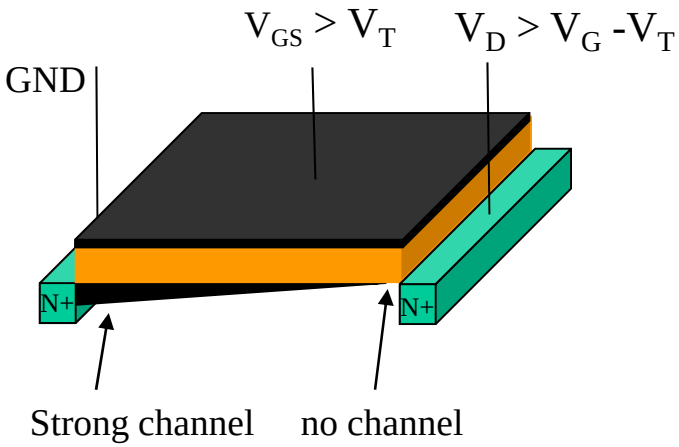
N-type transistor

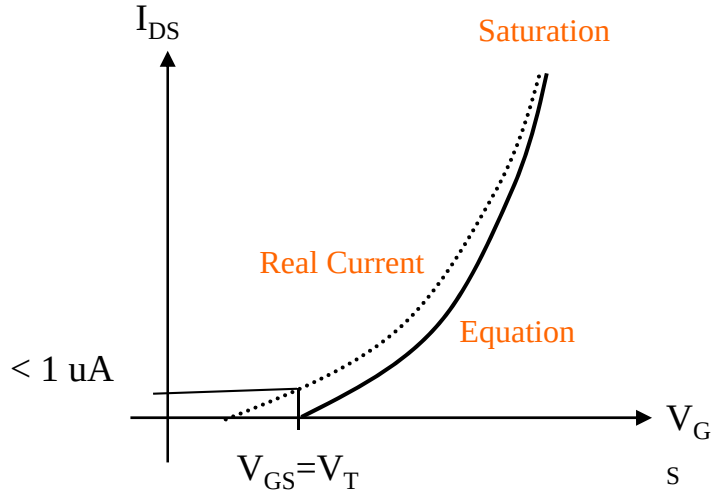
MOS Equation in **Saturation : $V_{GS}>V_T$**



Linear region: $I_D = \frac{W}{L}\mu_n C_{OX}\left(V_{GS} - V_T - 0.5V_{DS}\right)V_{DS}$

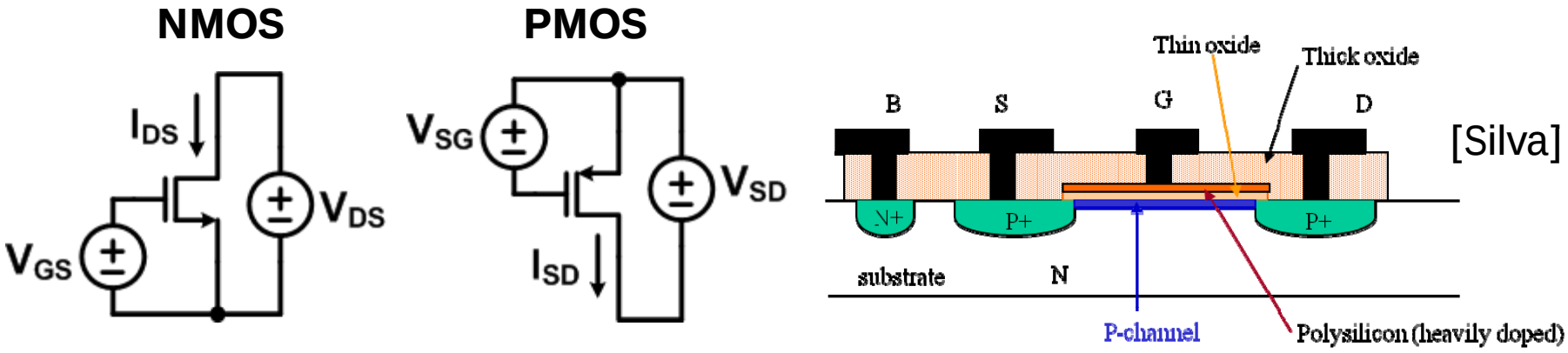
Saturation region: $I_D = \frac{W}{2L}\mu_n C_{OX}\left(V_{GS} - V_T\right)^2$





N-type transistor: saturation

What about the PMOS device?



- The current equations for the PMOS device <u>are the same</u> as the NMOS **EXCEPT** you swap the current direction and all the voltage polarities

	NMOS	**PMOS**
Linear:	$I_{DS} = \frac{W}{L}\mu_n C_{OX}\left(V_{GS} - V_{Tn} - 0.5V_{DS}\right)V_{DS}$	$I_{SD} = \frac{W}{L}\mu_p C_{OX}\left(V_{SG} - \lvert V_{Tp}\rvert - 0.5V_{SD}\right)V_{SD}$
Saturation:	$I_{DS} = \frac{W}{2L}\mu_n C_{OX}\left(V_{GS} - V_{Tn}\right)^2$	$I_{SD} = \frac{W}{2L}\mu_p C_{OX}\left(V_{SG} - \lvert V_{Tp}\rvert\right)^2$

MOS MODEL: SPICE LEVEL-II

- **Drain current, Triode region**

$$\textbf{NMOS}: I_{DS} = \frac{W}{L}\mu_n C_{OX}\left(V_{GS} - V_{Tn} - 0.5V_{DS}\right)V_{DS}$$

$$\textbf{PMOS}: I_{SD} = \frac{W}{L}\mu_p C_{OX}\left(V_{SG} - |V_{Tp}| - 0.5V_{SD}\right)V_{SD}$$

- **Drain Current, Saturation region**

$$\textbf{NMOS}: I_{DS} = \frac{W}{2L}\mu_n C_{OX}\left(V_{GS} - V_{Tn}\right)^2$$

$$\textbf{PMOS}: I_{SD} = \frac{W}{2L}\mu_p C_{OX}\left(V_{SG} - |V_{Tp}|\right)^2$$

- **Threshold voltage (zero bias)**

$$V_{T0} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F}$$

- **Threshold voltage**

$$V_T = V_{T0} + \gamma\left[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right] \Rightarrow V_{T0}\big|_{V_{SB}=0}$$

- **KP and γ (Spice Model)**

$$KP = \mu C_{OX}; \quad \gamma = \frac{\sqrt{2q\varepsilon_{si}N_{Bulk}}}{C_{OX}}$$

Next Time

- MOS Transistor Modeling
  - Small-Signal Model
  - Spice Models