ECEN474: (Analog) VLSI Circuit Design
Fall 2011

Lecture 1: Introduction

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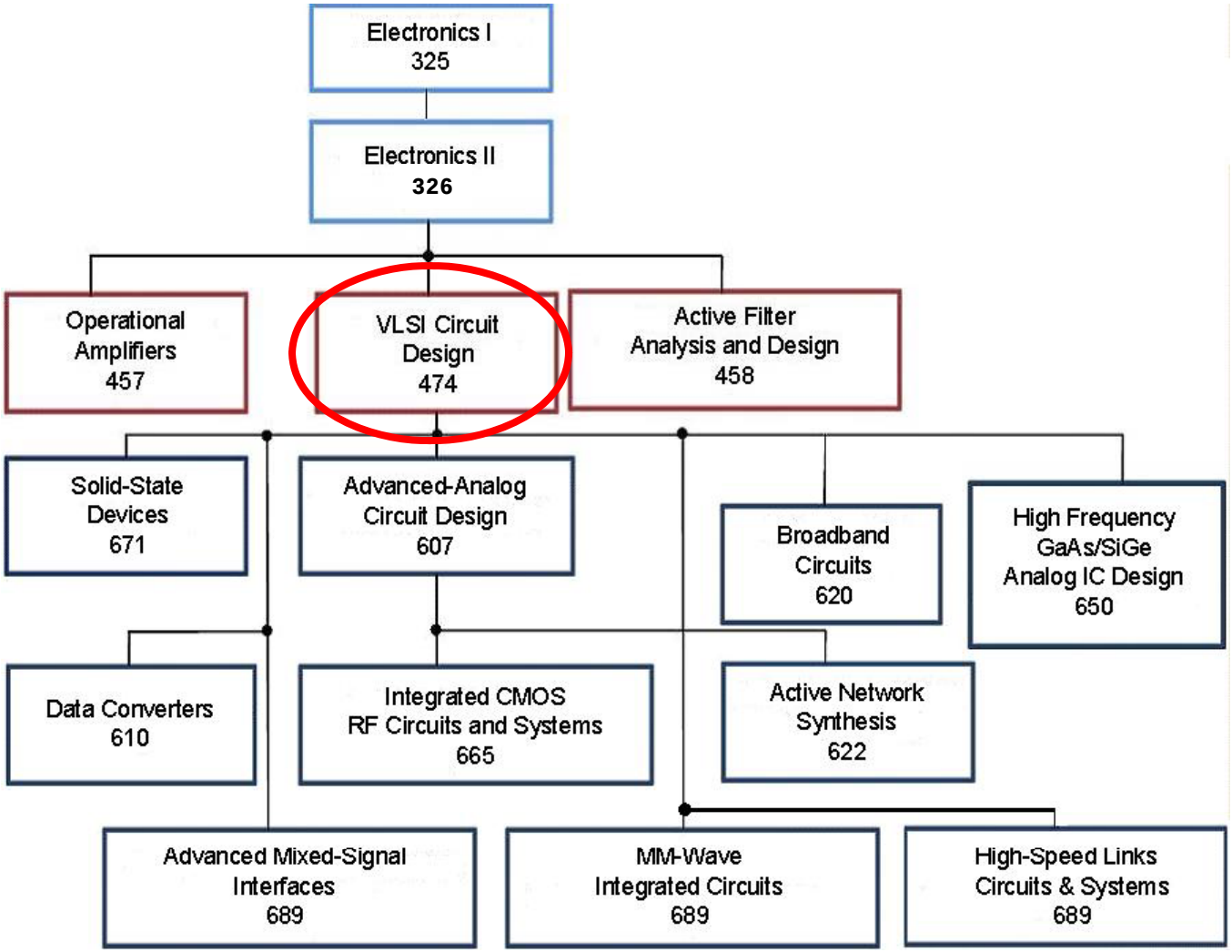
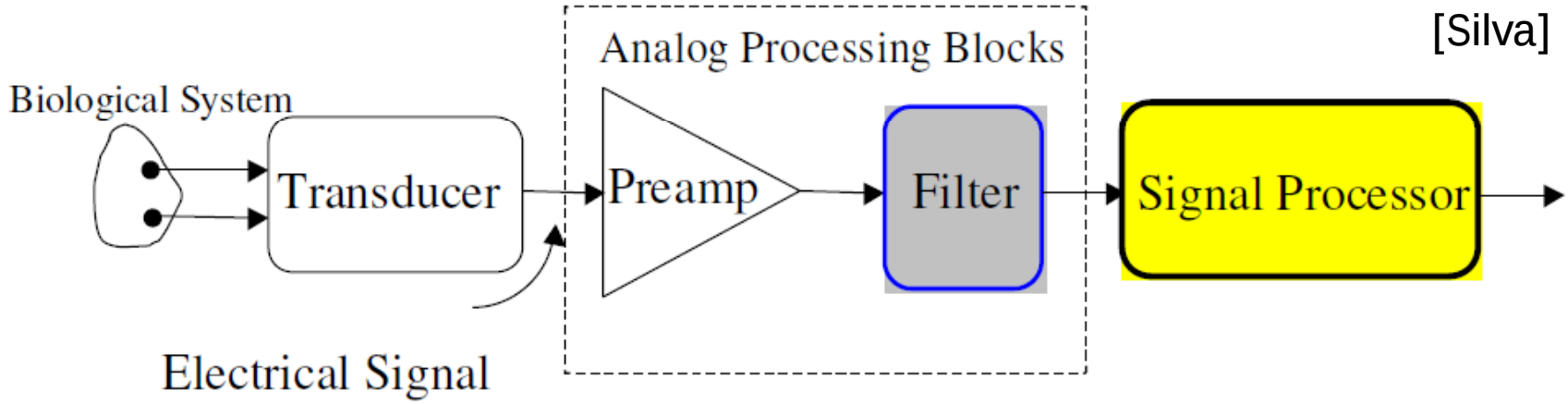
Analog & Mixed-Signal Center

Texas A&M University

Analog Circuit Sequence



Why is Analog Important?

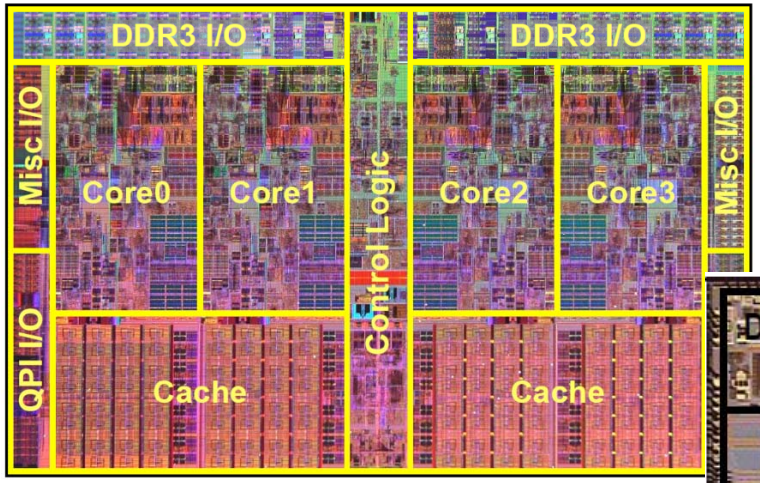


[Silva]

- Naturally occurring signals are analog
- Analog circuits are required to amplify and condition the signal for further processing
- Performance of analog circuits often determine whether the chip works or not
- Examples
  - Sensors and actuators (imagers, MEMS)
  - RF transceivers
  - Microprocessor circuits (PLL, high-speed I/O, thermal sensor)

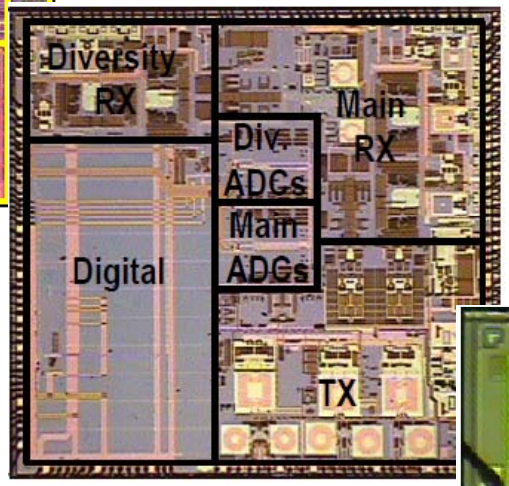
Integrated Circuits

[Bohr ISSCC 2009]



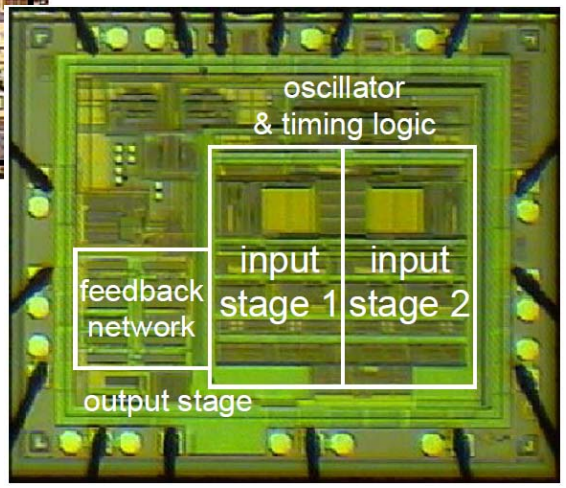
- 4-core Microprocessor (45nm CMOS)
  - Mostly Digital
  - Noteable analog blocks
    - PLL, I/O circuits, thermal sensor

[Sowlati ISSCC 2009]



- Cellular Transceiver (0.13μm CMOS)
  - Considerable analog & digital

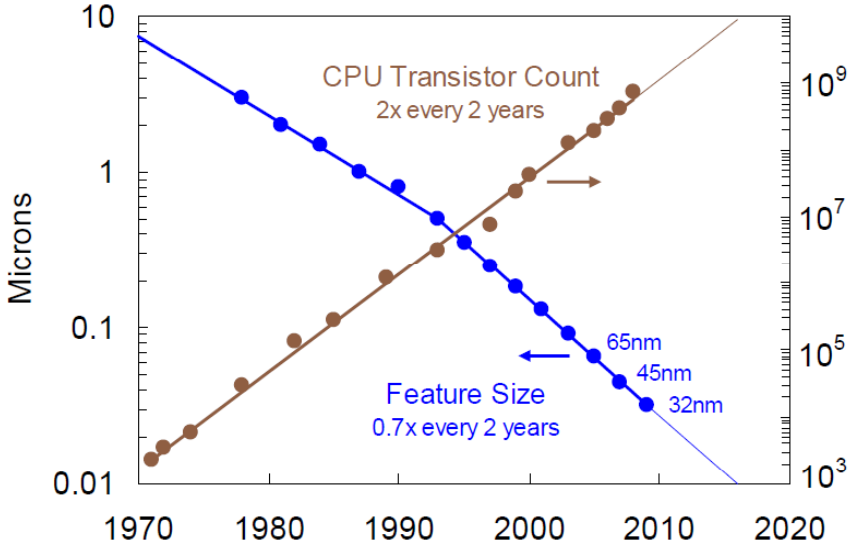
[Pertijs ISSCC 2009]

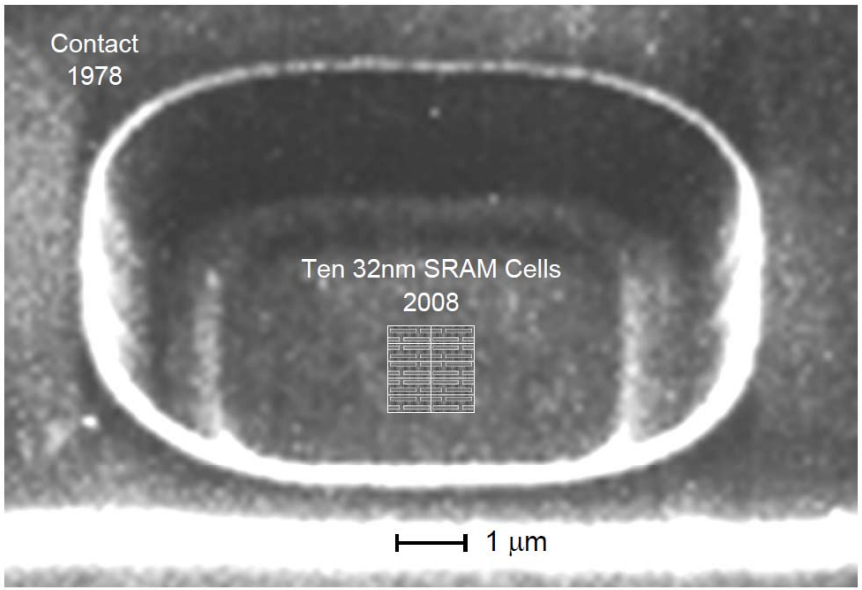


- Instrumentation Amplifier (0.5μm CMOS)
  - Mostly Analog
  - Some Digital Control Logic

The Power of CMOS Scaling

[Bohr ISSCC 2009]





- Scaling transistor dimensions allows for improved performance, reduced power, and reduced cost/transistor
- Assuming you can afford to build the fab
  - 32nm CMOS fab ~3-4 BILLION dollars

Course Topics

- CMOS technology
  - Active and passive devices
  - Layout techniques
- MOS circuit building blocks
  - Single-stage amplifiers, current mirrors, differential pairs
- Amplifiers and advanced circuit techiques

Course Goals

- Learn analog CMOS design approaches
  - Specification $\Rightarrow$ Circuit Topology $\Rightarrow$ Circuit Simulation $\Rightarrow$ Layout $\Rightarrow$ Fabrication
- Understand CMOS technology from a design perspective
  - Device modeling and layout techniques
- Use circuit building blocks to construct moderately complex analog circuits
  - Multi-stage amplifiers, filters, simple data converters, ...

Administrative

- Instructor:
  - Sebastian Hoyos
  - 315D WERC Bldg., 862-4253, hoyos@ece.tamu.edu
  - Office hours: MW 10:30am-12pm
- Lectures: MWF 9:10am-10am, ZACH 223B
- Class web page
  - http://www.ece.tamu.edu/~hoyos/ecen474.html

Class Material

- Textbook: *Design of Analog CMOS Integrated Circuits*, B. Razavi, McGraw-Hill, 2001
- References
  - *Analysis and Design of Analog Integrated Circuits*, P. Gray, R. Meyer, P. Hurst, and S. Lewis, John Wiley & Sons, 4th Edition, 2003.
  - Technical Papers
- Class notes
  - Posted on the web and will hand out hard copies in class

Grading

- Exams (60%)
  - Three midterm exams (20% each)
- Homework (10%)
  - Collaboration is allowed, but independent simulations and write-ups
  - Need to setup CADENCE simulation environment
  - Due at beginning of class
  - No late homework will be graded
- Laboratory (20%)
- Final Project (10%)
  - Groups of 1-2 students
  - Report and PowerPoint presentation required

Preliminary Schedule

Topic	Week
I. Introduction and MOS models	Week 1-4
II. CMOS Technologies and Layouts	
Review Session	**Sep. 28**
1st Exam	**Sep. 30**
III. Current Mirrors and Differential Pairs	Week 5-9
IV. Voltage References and Differential Pairs	
V. OTA Design (Part 1)	
Review Session	**Nov. 2**
2nd Exam	**Nov. 4**
VI. OTA Design (Part 2)	Week 10-14
VII. Miller OpAmp Design	
VIII. Advanced Topics	
Review Session	**Nov. 30**
3rd Exam	**Dec. 2**
Project Report Due	**Dec. 7**
Project Presentation	**Dec. 12**

- Dates may change with reasonable notice

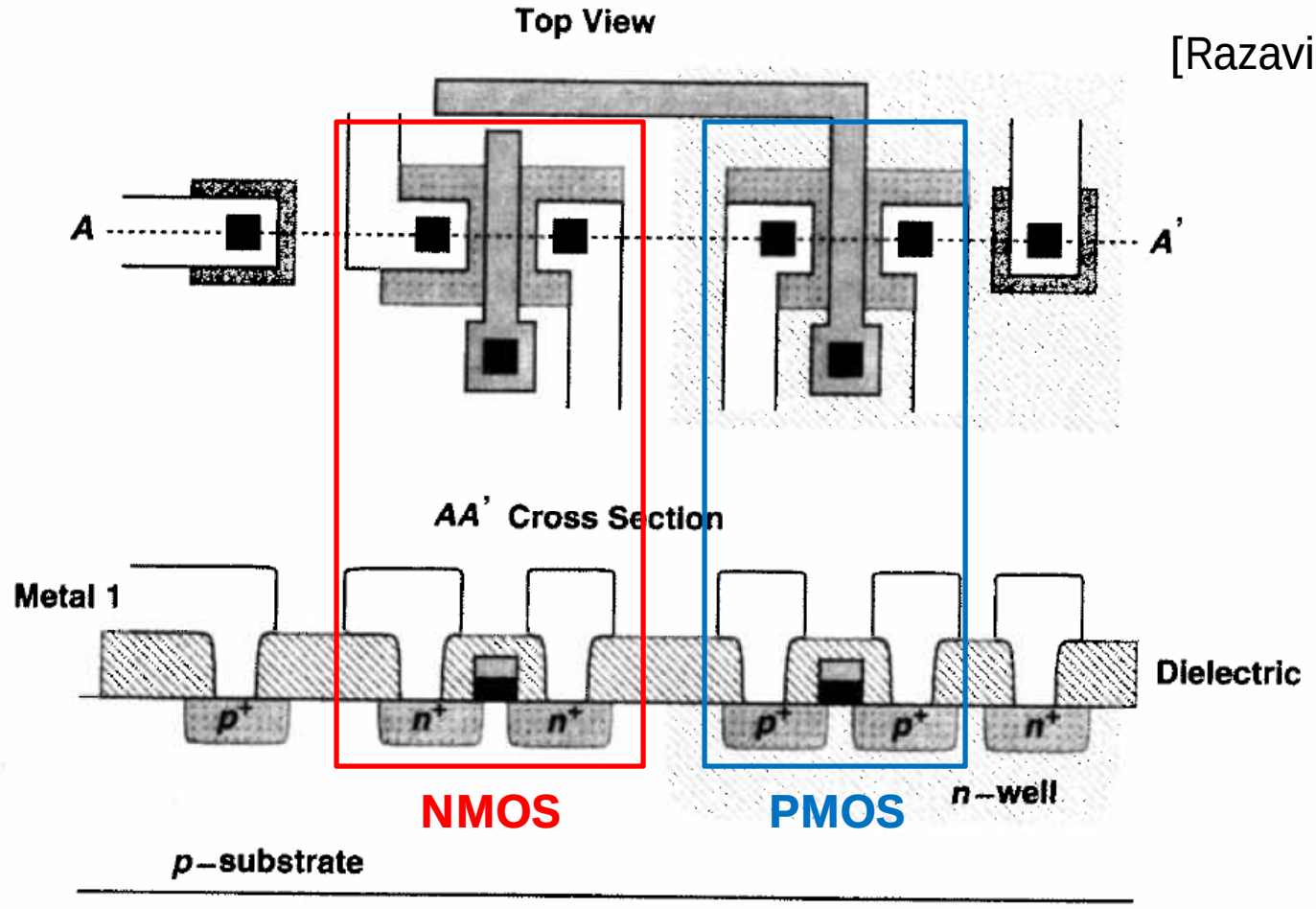
Reading

- Razavi's CMOS Book Chapter 1 and 2

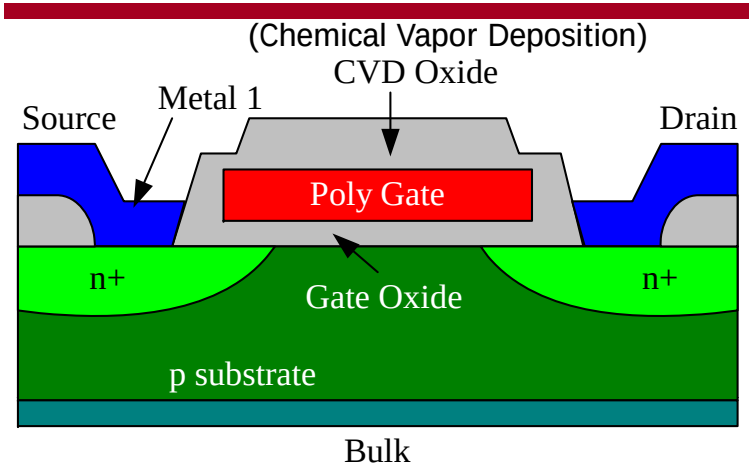
CMOS Technology Overview

- MOS Transistors
- Interconnect
- Diodes
- Resistors
- Capacitors
- Inductors
- Bipolar Transistors

CMOS Technology

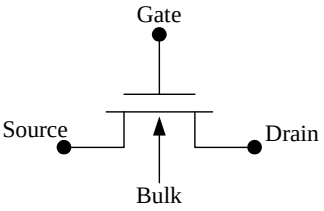


NMOS Transistor

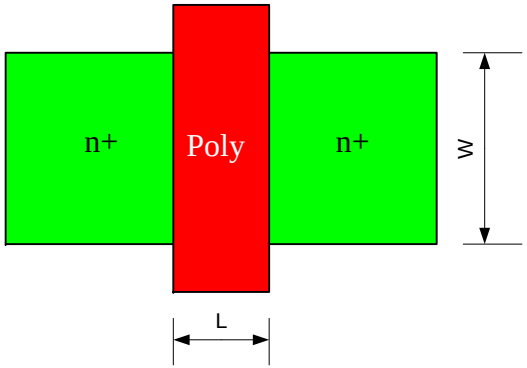


[Silva]

Cross Section

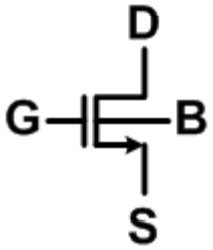


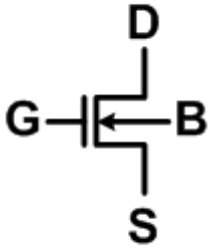
Circuit Symbol

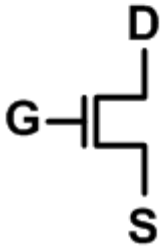


Top View

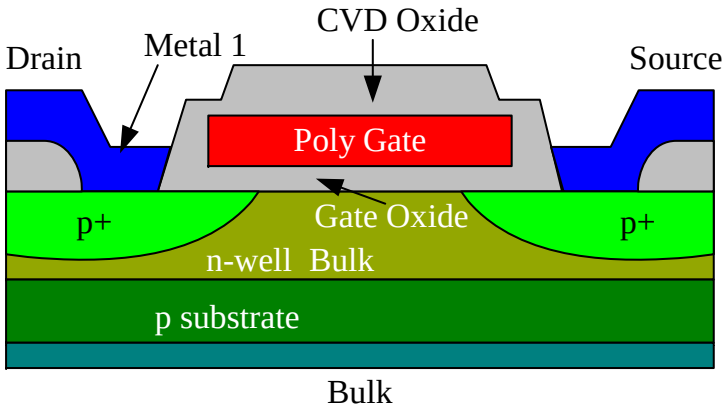
NMOS Symbols





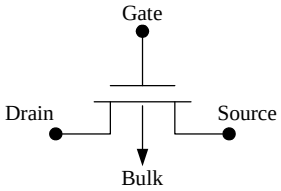


PMOS Transistor

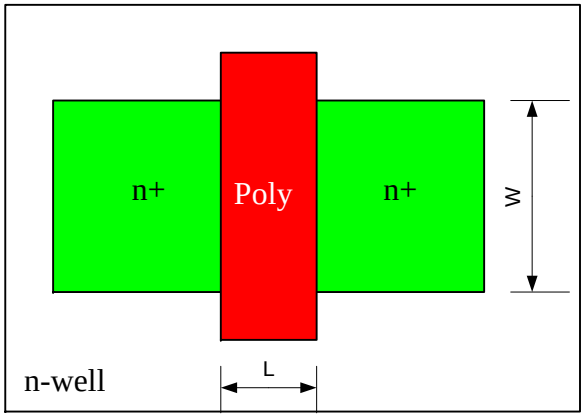


[Silva]

Cross Section

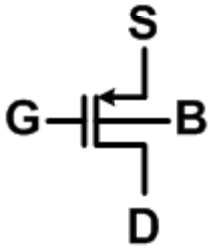


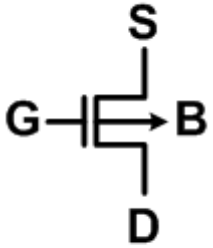
Circuit Symbol

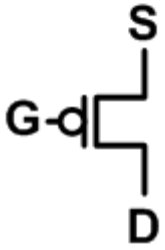


Top View

PMOS Symbols

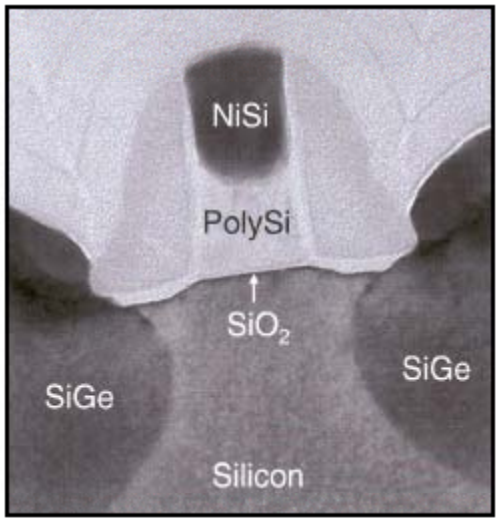






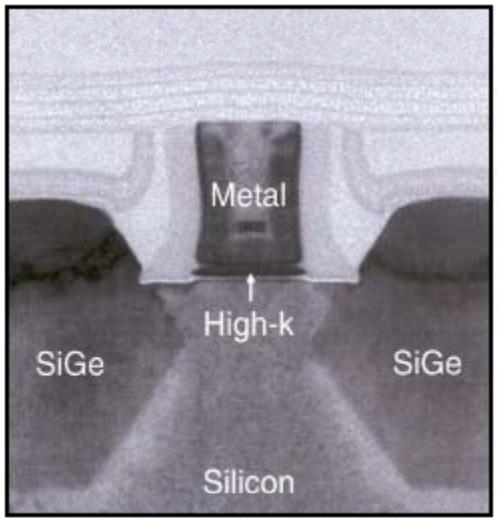
Today's CMOS Transistors

65 nm Transistor



SiO_2 dielectric
Polysilicon gate electrode

45 nm HK+MG [Bohr ISSCC 2009]



Hafnium-based dielectric
Metal gate electrode

- Today's transistors have advanced device structures
- Most advanced transistors are moving from poly-gates back to metal-gates
  - Allows for High-K gate dielectric and reduced gate leakage current

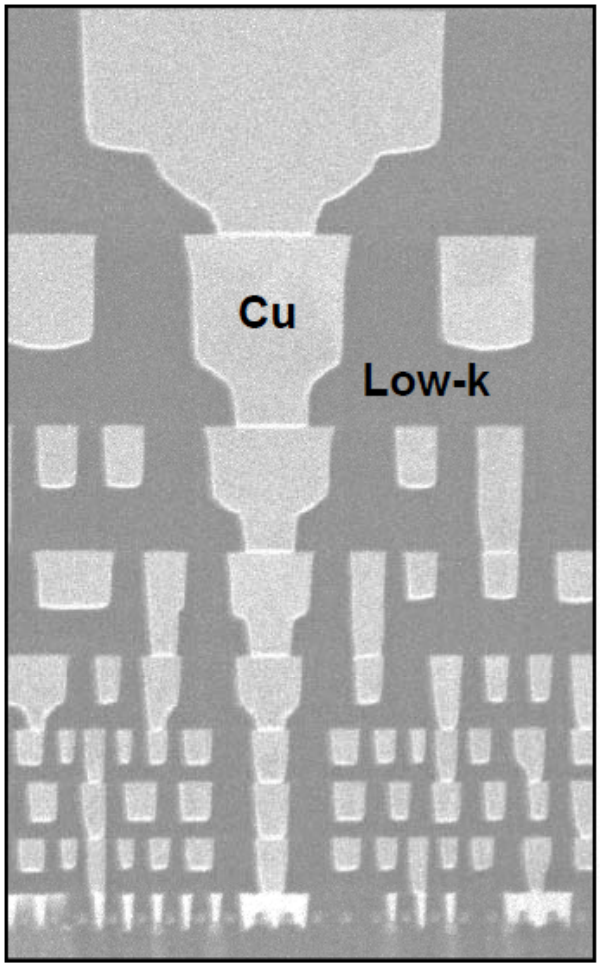
Interconnect (Wires)

Loose pitch + thick metal on upper layers

- High speed global wires
- Low resistance power grid

Tight pitch on lower layers

- Maximum density for local interconnects

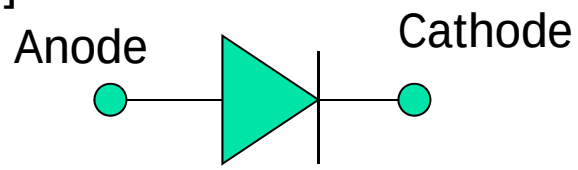


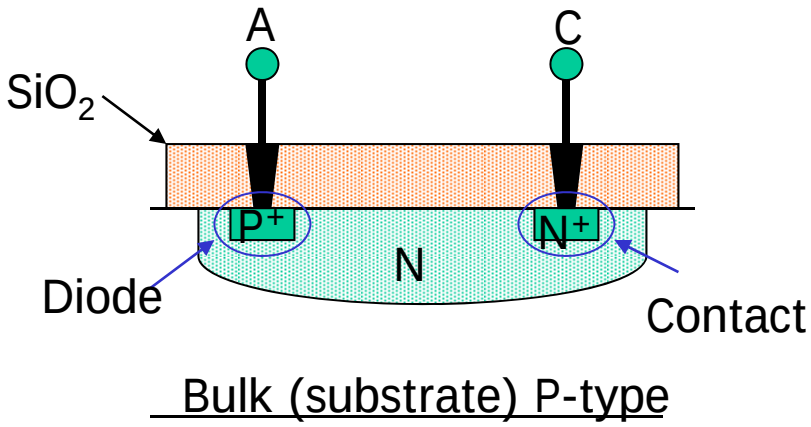
	Pitch (nm)
M8	810
M7	560
M6	360
M5	280
M4	240
M3	160
M2	160
M1	160

[Bohr ISSCC 2009]

Diodes

[Silva]





Typical values:

$P^+ = 10^{17}$-10^{19} acceptors /cm^3

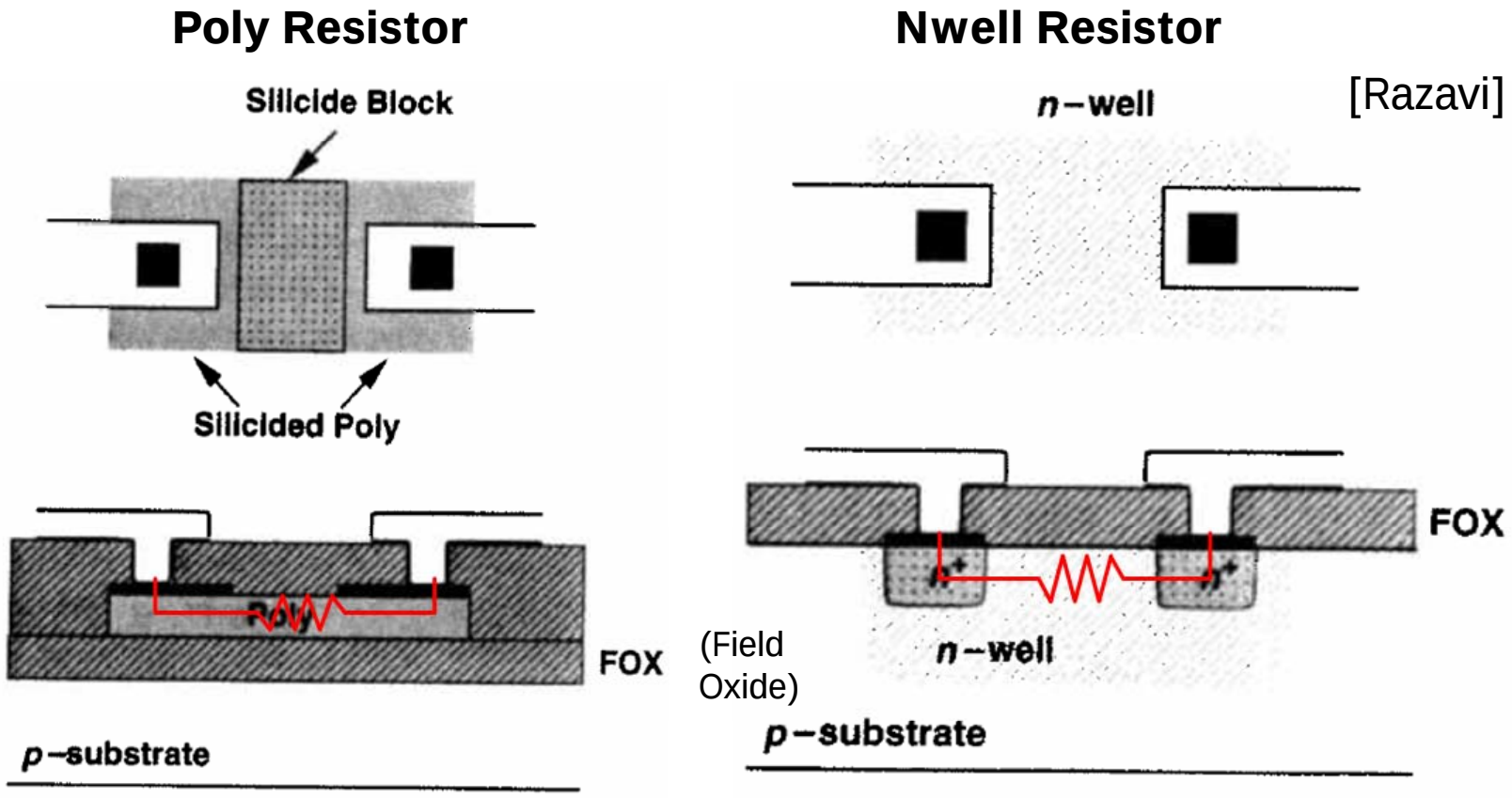
$P = 10^{15}$-10^{17} acceptors /cm^3

$N = 10^{16}$-10^{18} donors/cm^3

$N^+ = 10^{17}$-10^{19} donors/cm^3

Metal $\rightarrow$ 5×10^{22} electrons/cm^3

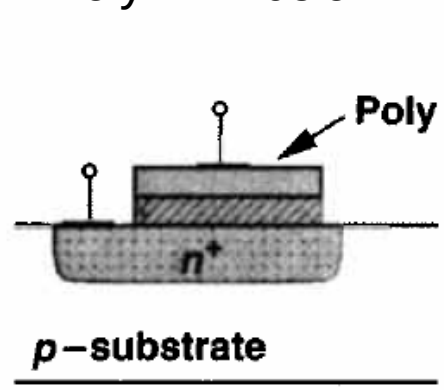
Resistors



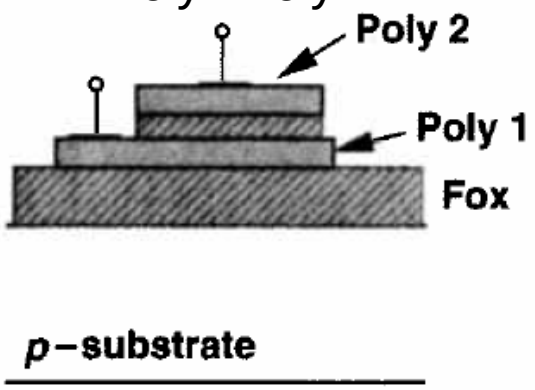
- Different resistor types have varying levels of accuracy and temperature and voltage sensitivities

Capacitors

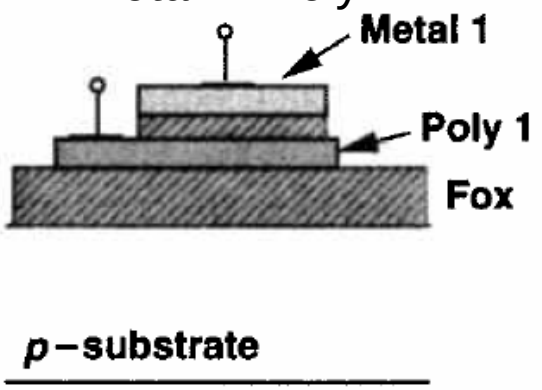
Poly - Diffusion



Poly - Poly

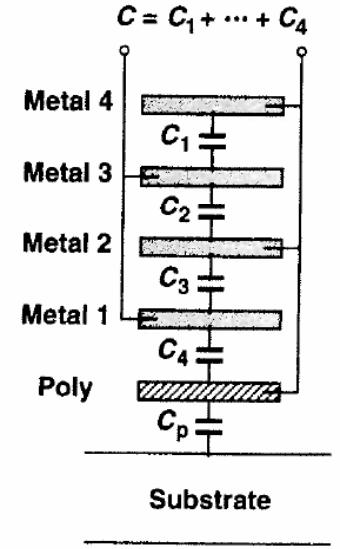


Metal1 - Poly

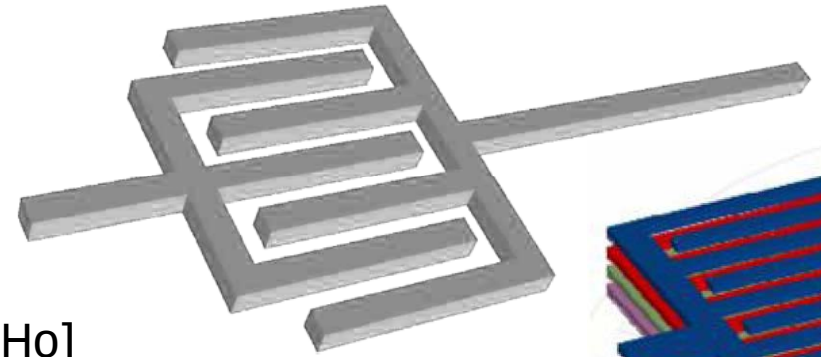


[Razavi]

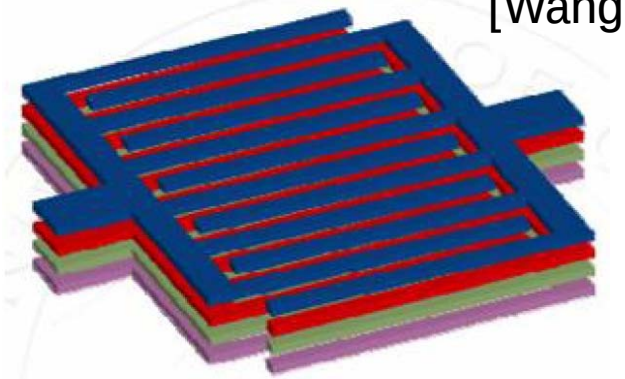
Vertical Metal “Sandwich”



Lateral Metal-Oxide-Metal (MOM)



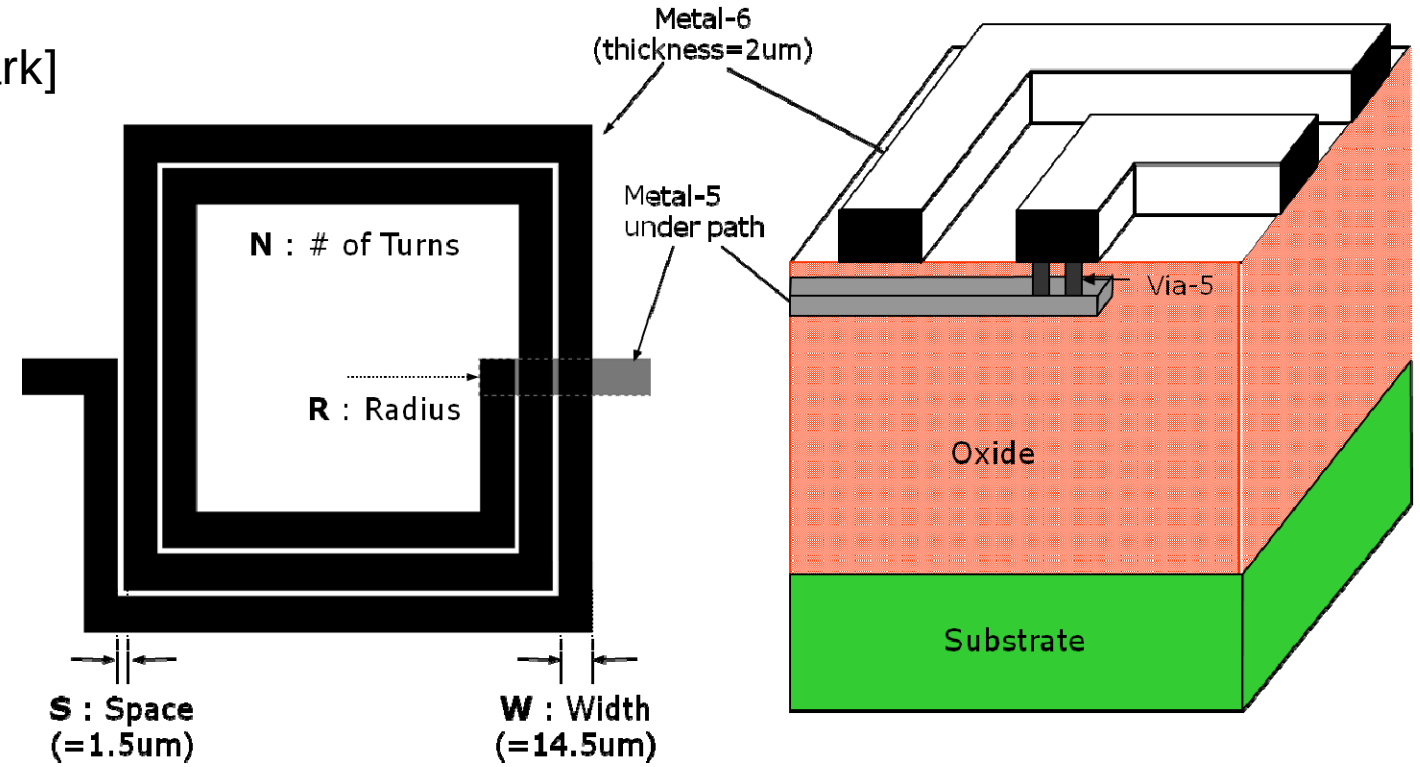
[Ho]



[Wang]

Inductors

[Silva/Park]

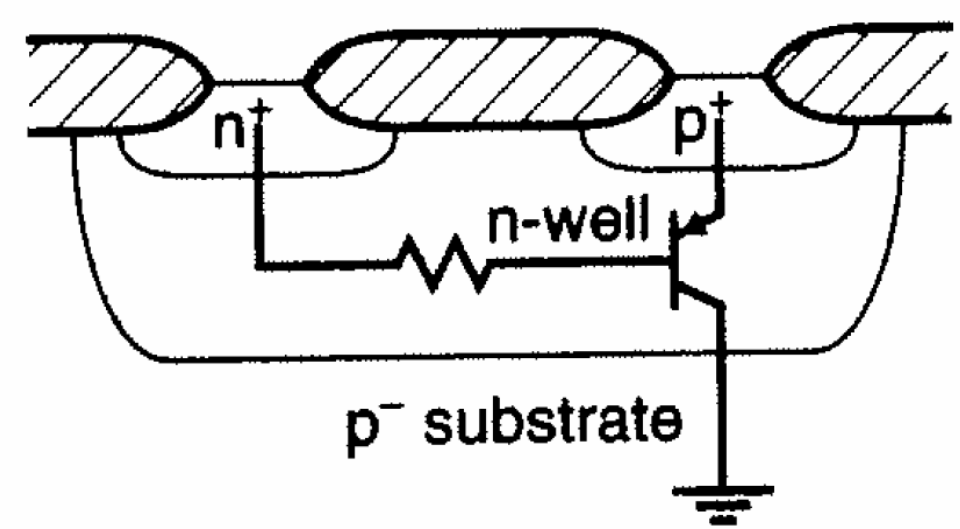


- Inductors are generally too big for widespread use in analog IC design
  - Can fit thousands of transistors in a typical inductor area (100μm x 100μm)
- Useful to extend amplifier bandwidth at zero power cost (but significant area cost)

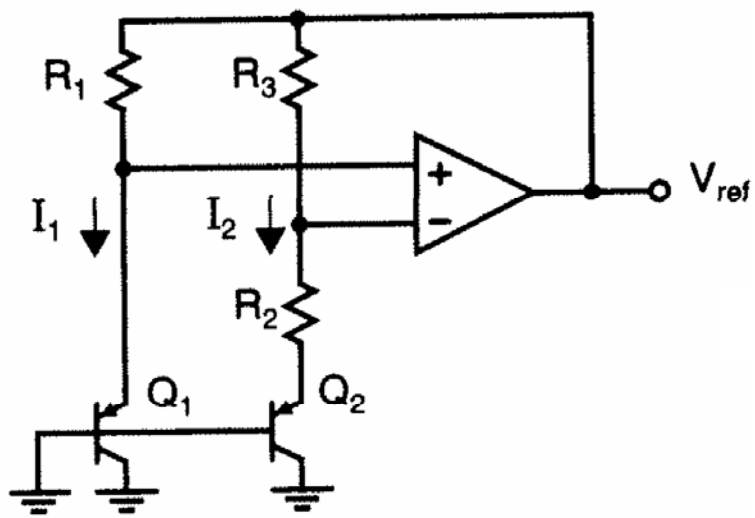
Bipolar Transistors – Vertical PNP

[Johns]

Vertical PNP



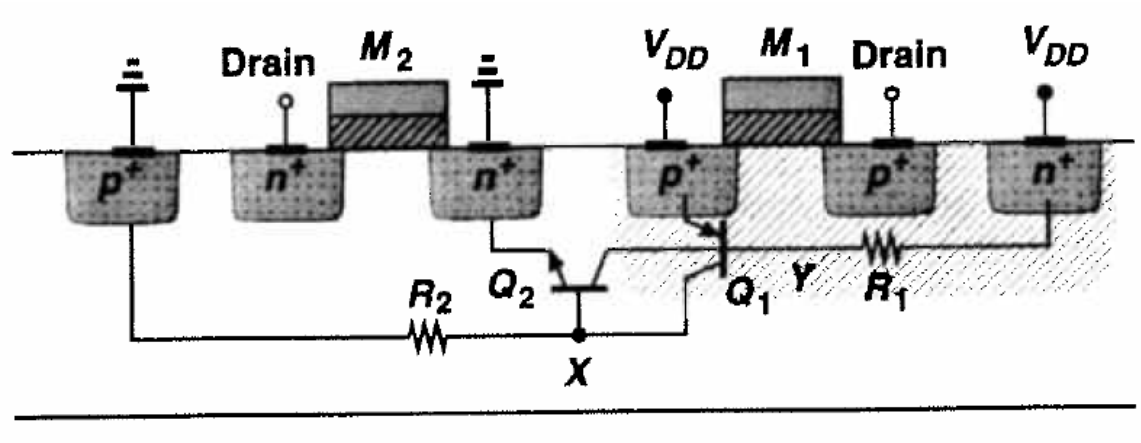
Bandgap Reference



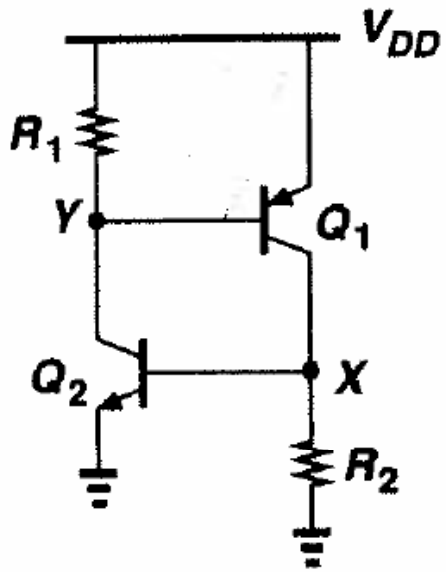
- Useful in a precise voltage reference circuit commonly implemented in ICs (Bandgap Reference)

Bipolar Transistors – Latchup

[Razavi]



Equivalent Circuit



- Potential for parasitic BJTs (Vertical PNP and Lateral NPN) to form a positive feedback loop circuit
- If circuit is triggered, due to current injected into substrate, then a large current can be drawn through the circuit and cause damage
- Important to minimize substrate and well resistance with many contacts/guard rings

Next Time

- MOS Transistor Modeling
  - DC I-V Equations
  - Small-Signal Model