

# ECEN 326 LAB 1

## Design of a Common-Emitter BJT Amplifier

### 1 Circuit Topology and Design Equations

General configuration of a single-supply common-emitter BJT amplifier is shown in Fig. 1.

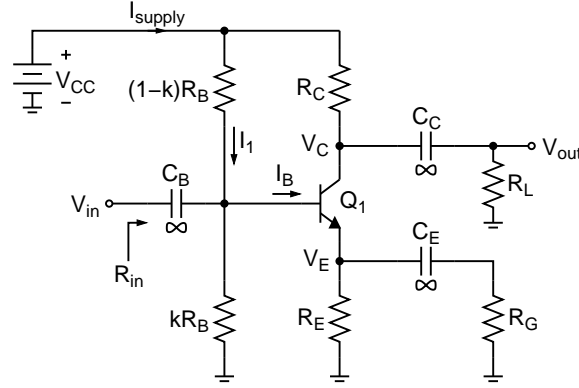


Figure 1: Common-Emitter BJT Amplifier

For  $\beta$ -insensitive DC biasing, the base current ( $I_B$ ) should be negligible compared to  $I_1$ :

$$I_B \ll I_1 \Rightarrow \frac{I_C}{\beta} \ll \frac{V_{CC}}{R_B} \Rightarrow N \frac{I_C}{\beta} = \frac{V_{CC}}{R_B} \Rightarrow R_B = \frac{\beta V_{CC}}{N I_C}, \quad N \geq 10 \quad (1)$$

Small-signal AC voltage gain ( $A_v$ ) can be expressed as

$$A_v = \left| \frac{v_{out}}{v_{in}} \right| = \frac{R_C \parallel R_L}{r_e + (R_E \parallel R_G)} \Rightarrow r_e + (R_E \parallel R_G) = \frac{R_C \parallel R_L}{A_v} \quad (2)$$

Input resistance of the amplifier ( $R_{in}$ ) is usually included in the given specifications. It can be calculated as

$$R_{in} = kR_B \parallel (1-k)R_B \parallel (\beta + 1)[r_e + (R_E \parallel R_G)] \approx k(1-k)R_B \parallel \beta[r_e + (R_E \parallel R_G)] \quad (3)$$

Substituting  $R_B$  from (1) and  $[r_e + (R_E \parallel R_G)]$  from (2) into (3) results in

$$R_{in} = \left( k(1-k) \frac{\beta V_{CC}}{N I_C} \right) \parallel \left( \beta \frac{R_C \parallel R_L}{A_v} \right) = \frac{\beta}{\frac{N I_C}{k(1-k)V_{CC}} + \frac{A_v}{R_C \parallel R_L}} \quad (4)$$

To maximize the available output swing, load-line analysis needs to be performed. Assume that the transistor's DC operating point is set to  $(I_C, V_{CE})$ . The following equation can be obtained from the DC equivalent circuit of Fig. 1

$$V_{CC} = I_C R_C + V_{CE} + V_E \Rightarrow V_{CE} = V_{CC} - I_C R_C - V_E \quad (5)$$

AC load line, which shows the relationship between the AC signals  $i_c$  and  $v_{ce}$ , passes through the DC bias point  $(I_C, V_{CE})$ . The slope of the line depends on the AC resistance at the collector and emitter terminals. For the common-emitter amplifier circuit in Fig. 1, the slope can be found as

$$\frac{\Delta i_c}{\Delta v_{ce}} = - \frac{1}{(R_C \parallel R_L) + (R_E \parallel R_G)} \quad (6)$$

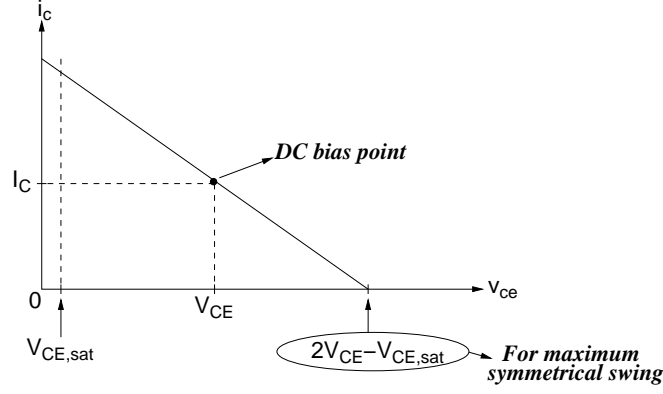


Figure 2: AC load line

Therefore, the load line equation can be obtained as

$$\frac{i_c - I_C}{v_{ce} - V_{CE}} = -\frac{1}{(R_C \parallel R_L) + (R_E \parallel R_G)} \quad (7)$$

To obtain the maximum symmetrical swing, the DC bias point should be at the middle of the available region. Since the minimum value for  $v_{ce}$  is  $V_{CE,sat}$ , the maximum value of  $v_{ce}$  corresponding to  $i_c = 0$  should be  $(2V_{CE} - V_{CE,sat})$ , as shown in Fig. 2. Evaluating the load-line equation at the point  $(i_c, v_{ce}) = (0, 2V_{CE} - V_{CE,sat})$ ,

$$\frac{0 - I_C}{2V_{CE} - V_{CE,sat} - V_{CE}} = -\frac{1}{(R_C \parallel R_L) + (R_E \parallel R_G)} \quad (8)$$

which can be arranged as

$$I_C[(R_C \parallel R_L) + (R_E \parallel R_G)] = V_{CE} - V_{CE,sat} \quad (9)$$

Substituting  $V_{CE}$  from (5) into (9) results in

$$I_C[(R_C \parallel R_L) + (R_E \parallel R_G)] = V_{CC} - I_C R_C - V_E - V_{CE,sat} \quad (10)$$

which can be arranged as

$$I_C = \frac{V_X}{R_C + (R_C \parallel R_L) + (R_E \parallel R_G)} \quad (11)$$

where

$$V_X = V_{CC} - V_E - V_{CE,sat} \quad (12)$$

From (2),  $A_v \gg 1$  implies  $(R_C \parallel R_L) \gg (R_E \parallel R_G)$ . Therefore, (11) can be simplified as

$$I_C \approx \frac{V_X}{R_C + (R_C \parallel R_L)} \quad (13)$$

0-to-peak voltage swing can be calculated as

$$V_{sw} = I_C(R_C \parallel R_L) = \frac{V_X}{2 + \frac{R_C}{R_L}} \quad (14)$$

Substituting  $I_C$  in (13) into (4),  $R_{in}$  can be expressed as

$$R_{in} = \frac{\beta(R_C \parallel R_L)}{\frac{NV_X}{k(1-k)V_{CC}} \frac{1}{2 + \frac{R_C}{R_L}} + A_v} \quad (15)$$

## 2 Design Procedure

1.  $V_{CC}$ ,  $V_{CE,sat}$  and  $\beta$  should be given together with the design specifications, which usually include  $R_{in}$ ,  $A_v$ , 0-to-peak output swing ( $V_{sw}$ ), and  $R_L$ . In addition, the design should be insensitive to variations in  $\beta$  and  $V_{BE}$ .
2. First, choose the value of  $V_E$ . Increasing  $V_E$  results in more stable bias current in the presence of  $V_{BE}$  variations, however it decreases the available voltage swing at the collector. If the resistor  $R_E$  is replaced with a DC current source,  $V_E$  should be sufficiently large to allow proper operation of the source.
3. Calculate  $V_X$  and  $k$  as follows

$$V_X = V_{CC} - V_{CE,sat} - V_E \quad , \quad k = \frac{V_E + 0.7}{V_{CC}}$$

Also choose  $N$  such that  $N \geq 10$ .

4. Determine the minimum value of  $R_C$  using the specification for the desired input resistance ( $R_{in,d}$ ):

$$\frac{\frac{\beta(R_C \parallel R_L)}{NV_X}}{\frac{k(1-k)V_{CC}}{2 + \frac{R_C}{R_L}} + A_v} \geq R_{in,d}$$

which can be arranged as

$$R_C^2(\beta R_L - R_{in,d}A_v) + R_C(2\beta R_L - 3R_{in,d}A_v - QR_{in,d})R_L - R_L^2R_{in,d}(Q + 2A_v) \geq 0$$

where

$$Q = \frac{NV_X}{k(1-k)V_{CC}}$$

5. Determine the maximum value of  $R_C$  using the specification for the desired output voltage swing ( $V_{sw,d}$ ):

$$\frac{V_X}{2 + \frac{R_C}{R_L}} \geq V_{sw,d}$$

which can be arranged as

$$R_C \leq R_L \left( \frac{V_X}{V_{sw,d}} - 2 \right)$$

6. Choose  $R_C$ , then calculate  $I_C$

$$I_C \approx \frac{V_X}{R_C + (R_C \parallel R_L)}$$

7. Calculate  $R_B$  and  $R_E$

$$R_B = \frac{\beta V_{CC}}{NI_C} \quad , \quad R_E = \frac{V_E}{I_C}$$

8. Find  $R_G$  from

$$r_e + (R_E \parallel R_G) = \frac{R_C \parallel R_L}{A_v}$$

which can be arranged as

$$R_G = \frac{1}{\frac{1}{\left( \frac{R_C \parallel R_L}{A_v} - r_e \right)} - \frac{1}{R_E}}$$

### 3 Pre-Lab

Using a Q2N2222 BJT, design a common-emitter amplifier with the following specifications:

$$\begin{array}{lll} V_E \geq 1 \text{ V} & R_{in} \geq 5 \text{ k}\Omega & \text{0-to-peak unclipped swing at } V_{out} \geq 1.6 \text{ V} \\ V_{CC} = 5 \text{ V} & |A_v| = 40 & \text{Operating frequency: 5 kHz} \\ R_L = 10 \text{ k}\Omega & I_{supply} \leq 1.5 \text{ mA} & \end{array}$$

1. Show all your calculations and final component values.
2. Verify your results using PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using PSPICE, perform Fourier analysis and determine the input and the output signal amplitudes resulting in 5% total harmonic distortion (THD) at the output. Submit transient and Fourier plots, and the distortion data from the output file.
4. Be prepared to discuss your design at the beginning of the lab period with your TA.

### 4 Lab Procedure

1. Construct the common-emitter amplifier you designed in the pre-lab.
2. Measure  $I_C$ ,  $V_E$ ,  $V_C$  and  $V_B$ . If any DC bias value is significantly different than the one obtained from Pspice simulations, modify your circuit to get the desired DC bias before you move onto the next step.
3. Measure  $I_{supply}$ ,  $A_v$ ,  $R_{in}$ , and  $R_{out}$ .
4. Measure the maximum unclipped output signal amplitude.
5. Apply the input signal level resulting in 5% THD at the output, and measure the input and output signal amplitudes.
6. Prepare a data sheet showing your simulated and measured values.
7. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.

# ECEN 326 LAB 2

## Design of a Three-Stage BJT Amplifier

### 1 Circuit Topology and Design Equations

Figure 1 shows the three-stage amplifier to be designed in this lab. The first stage is a common-emitter amplifier, which is followed by a common-base stage. This combination is known as the cascode amplifier. An emitter follower is added as the final stage.

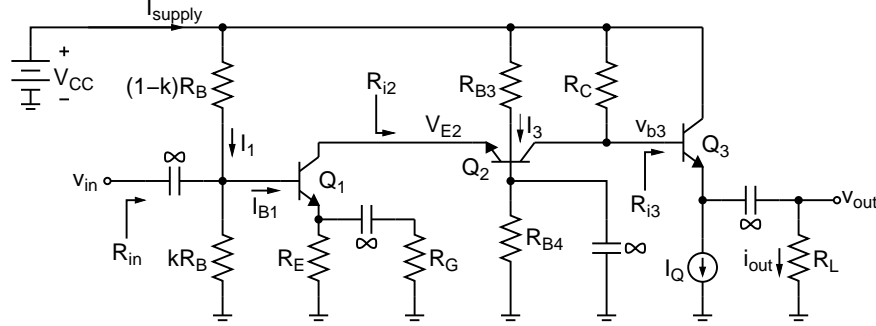


Figure 1: Cascode amplifier with an emitter follower

For  $\beta$ -insensitive DC biasing, the base current of  $Q_1$  ( $I_{B1}$ ) should be negligible compared to  $I_1$ :

$$I_{B1} \ll I_1 \Rightarrow \frac{I_{C1}}{\beta} \ll \frac{V_{CC}}{R_B} \Rightarrow N \frac{I_{C1}}{\beta} = \frac{V_{CC}}{R_B} \Rightarrow R_B = \frac{\beta V_{CC}}{N I_{C1}}, \quad N \geq 10 \quad (1)$$

Small-signal AC voltage gain ( $A_v$ ) can be expressed as

$$A_v = \left| \frac{v_{out}}{v_{in}} \right| = \frac{R_{i2}}{r_{e1} + (R_E \parallel R_G)} \frac{R_C \parallel R_{i3}}{R_{i2}} A_F \Rightarrow r_{e1} + (R_E \parallel R_G) = \frac{R_C \parallel R_{i3}}{A_v} A_F \quad (2)$$

where

$$A_F = \frac{v_{out}}{v_{b3}} = \frac{R_L}{r_{e3} + R_L} \quad (3)$$

$$R_{i3} = (\beta + 1)(r_{e3} + R_L) \quad (4)$$

Input resistance of the amplifier ( $R_{in}$ ) can be calculated as

$$R_{in} = kR_B \parallel (1-k)R_B \parallel (\beta + 1)[r_{e1} + (R_E \parallel R_G)] \approx k(1-k)R_B \parallel \beta[r_{e1} + (R_E \parallel R_G)] \quad (5)$$

Substituting  $R_B$  from (1) and  $[r_{e1} + (R_E \parallel R_G)]$  from (2) into (5) results in

$$R_{in} = \left( k(1-k) \frac{\beta V_{CC}}{N I_{C1}} \right) \parallel \left( \beta \frac{R_C \parallel R_{i3}}{A_v} A_F \right) = \frac{\beta}{\frac{N I_{C1}}{k(1-k)V_{CC}} + \frac{A_v}{(R_C \parallel R_{i3})A_F}} \quad (6)$$

The small-signal AC voltage gain from  $v_{in}$  to  $v_{e2}$  is less than unity. Therefore, the AC signal swing at  $v_{e2}$  can be assumed to be limited by the maximum input signal amplitude ( $V_{i,max}$ ), which can be calculated by dividing the required output swing to the gain specification. To avoid clipping at  $v_{e2}$ , the DC bias at  $V_{E2}$  can be chosen as

$$V_{E2} \geq V_{E1} + V_{CE,sat} + V_{i,max} \quad (7)$$

To maximize the available output swing, load-line analysis needs to be performed. Assume that  $Q_2$ 's DC operating point is set to  $(I_{C2}, V_{CE2})$ . From Fig. 1

$$V_{CC} \approx I_{C2}R_C + V_{CE2} + V_{E2} \Rightarrow V_{CE2} = V_{CC} - I_{C2}R_C - V_{E2} \quad (8)$$

Please note that the above expression is valid only if  $I_{C2} \gg I_{B3}$ . Since  $I_{C3}$  is usually a large current, this requirement usually determines the minimum amount of  $I_{C2}$ . AC load line equation for  $Q_2$  (see Fig. 2) can be obtained as

$$\frac{i_{c2} - I_{C2}}{v_{ce2} - V_{CE2}} \approx -\frac{1}{R_C \parallel R_{i3}} \quad (9)$$

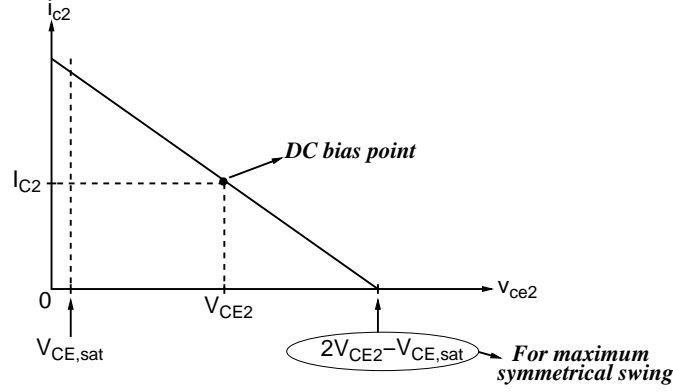


Figure 2: AC load line

Evaluating the load-line equation at the point  $(i_{c2}, v_{ce2}) = (0, 2V_{CE2} - V_{CE,sat})$ ,

$$\frac{0 - I_{C2}}{2V_{CE2} - V_{CE,sat} - V_{CE2}} = -\frac{1}{R_C \parallel R_{i3}} \quad (10)$$

which can be arranged as

$$I_{C2}(R_C \parallel R_{i3}) = V_{CE2} - V_{CE,sat} \quad (11)$$

Substituting  $V_{CE2}$  from (8) into (11) results in

$$I_{C2} = \frac{V_X}{R_C + (R_C \parallel R_{i3})} = I_{C1} \quad (12)$$

where

$$V_X = V_{CC} - V_{E2} - V_{CE,sat} \quad (13)$$

0-to-peak voltage swing at the output can be calculated as

$$V_{sw} = I_{C2}(R_C \parallel R_{i3})A_F = \frac{V_X}{R_C} A_F \frac{1}{2 + \frac{R_C}{R_{i3}}} \quad (14)$$

Substituting  $I_{C1}$  in (12) into (6),  $R_{in}$  can be expressed as

$$R_{in} = \frac{\beta(R_C \parallel R_{i3})}{\frac{NV_X}{k(1-k)V_{CC}} \frac{1}{2 + \frac{R_C}{R_{i3}}} + \frac{A_v}{A_F}} \quad (15)$$

The final stage is an emitter follower, which should be designed to deliver the specified voltage swing to the load. Assuming large signals, KCL at the output node results in

$$i_{C3} = I_Q + i_{out} \quad (16)$$

where  $i_{out}$  is a sine wave and  $I_Q$  is a DC current. Since  $i_{C3} > 0$  for  $Q_3$  to be active,  $i_{out}$  cannot be lower than  $-I_Q$  during the negative cycle of the sine wave. Using the specifications for the output swing and load resistor,  $I_Q$  can be determined from

$$I_Q \geq \frac{\text{0-to-peak output swing}}{R_L} \quad (17)$$

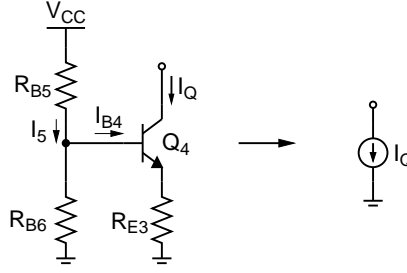


Figure 3: DC current source

The current source can be designed using the circuit in Fig. 3, where  $I_Q$  can be calculated from

$$I_Q = \frac{V_{CC} \frac{R_{B6}}{R_{B5} + R_{B6}} - 0.7}{R_{E3}} \quad (18)$$

In general, all DC bias points in the circuit should be insensitive to variations in  $\beta$ . Therefore,  $R_{B3}$ ,  $R_{B4}$ ,  $R_{B5}$  and  $R_{B6}$  should be chosen such that:

$$I_{B2} \ll I_3 \quad (19)$$

$$I_{B4} \ll I_5 \quad (20)$$

## 2 Design Procedure

1. Choose  $I_Q$  such that (17) is satisfied.
2. Since  $I_{C3} = I_Q$ , calculate  $A_F$  and  $R_{i3}$  from (3) and (4).
3. Choose the value of  $V_{E1}$ , and then find  $V_{E2}$  from (7).
4. Calculate  $V_X$  from (13), and  $k$  from  $k = (V_{E1} + 0.7)/V_{CC}$ . Also choose  $N$  such that  $N \geq 10$ .
5. Determine the minimum value of  $R_C$  using the specification for the desired input resistance ( $R_{in,d}$ ):

$$\frac{\beta(R_C \parallel R_{i3})}{\frac{NV_X}{k(1-k)V_{CC}} \frac{1}{2 + \frac{R_C}{R_{i3}}} + \frac{A_v}{A_F}} \geq R_{in,d}$$

which can be arranged as

$$R_C^2 \left( \beta R_{i3} - R_{in,d} \frac{A_v}{A_F} \right) + R_C \left( 2\beta R_{i3} - 3R_{in,d} \frac{A_v}{A_F} - QR_{in,d} \right) R_{i3} - R_{i3}^2 R_{in,d} \left( Q + 2 \frac{A_v}{A_F} \right) \geq 0$$

where

$$Q = \frac{NV_X}{k(1-k)V_{CC}}$$

6. Determine the maximum value of  $R_C$  using the specification for the desired output voltage swing ( $V_{sw,d}$ ):

$$\frac{V_X}{2 + \frac{R_C}{R_{i3}}} A_F \geq V_{sw,d} \Rightarrow R_C \leq R_{i3} \left( \frac{V_X A_F}{V_{sw,d}} - 2 \right)$$

7. Choose  $R_C$ , then calculate  $I_{C2} = I_{C1}$  from (12). Make sure that  $I_{C2} \gg I_Q/\beta$ , if not, repeat the steps above (as many steps as necessary) to obtain an acceptable  $I_{C2}$ .

8. Calculate  $R_B$  and  $R_E$

$$R_B = \frac{\beta V_{CC}}{N I_{C1}} \quad , \quad R_E = \frac{V_E}{I_{C1}}$$

9. Find  $R_G$  from (2), which can be arranged as

$$R_G = \frac{1}{\frac{1}{\left(\frac{R_C \parallel R_{i3}}{A_v} A_F - r_{e1}\right)} - \frac{1}{R_E}}$$

10. Choose  $V_{E4}$  such that  $V_{E4} + V_{CE,sat} \leq V_{E3} - V_{out,0-to-peak}$ , then calculate  $R_{E3} \approx V_{E4}/I_Q$ .

11. Find  $R_{B3}$ ,  $R_{B4}$ ,  $R_{B5}$  and  $R_{B6}$  while (19) and (20) are satisfied.

### 3 Pre-Lab

Design the 3-stage amplifier in Fig. 1 with the following specifications:

$$\begin{array}{lll} V_{CC} = 5 \text{ V} & R_L = 100 \Omega & \text{Operating frequency: 5 kHz} \\ |A_v| = 30 & R_{in} \geq 3k \Omega & \text{Zero-to-peak un-clipped swing at } V_{out} \geq 1.5 \text{ V} \\ I_{supply} \leq 20 \text{ mA} & V_{E1} \geq 1 \text{ V} & V_{E4} \geq 0.5 \text{ V} \end{array}$$

Use Q2N3904 for  $Q_1$  and  $Q_2$ , and Q2N2222 for  $Q_3$  and  $Q_4$ .

1. Show all your calculations, design procedure, and final component values.
2. Verify your results using PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using PSPICE, perform Fourier analysis and determine the input and the output signal amplitudes resulting in 5% total harmonic distortion (THD) at the output. Submit transient and Fourier plots, and the distortion data from the output file.
4. Be prepared to discuss your design at the beginning of the lab period with your TA.

### 4 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.
2. Measure  $I_C$ ,  $V_C$ ,  $V_B$  and  $V_E$  for all transistors. If any DC bias value is significantly different than the one obtained from Pspice simulations, modify your circuit to get the desired DC bias before you move onto the next step.
3. Measure  $I_{supply}$ ,  $A_v$  and  $R_{in}$ .
4. Measure the maximum un-clipped output signal amplitude.
5. Apply the input signal level resulting in 5% THD at the output, and measure the input and output signal amplitudes.
6. Prepare a data sheet showing your simulated and measured values.
7. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.

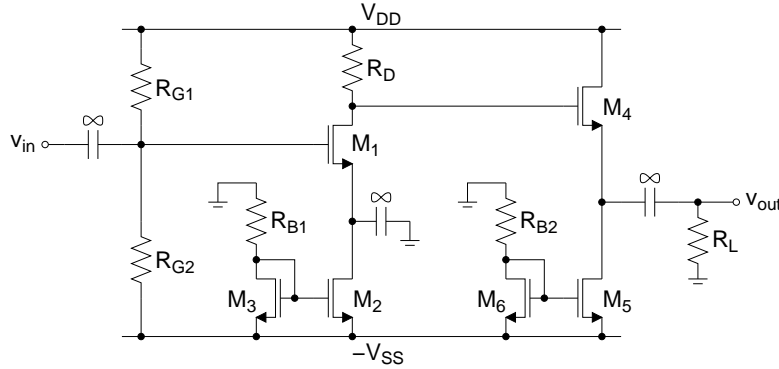


## ECEN 326 LAB 3

# Design of a Common-Source MOSFET Amplifier with a Source Follower

## 1 Circuit Topology and Design Equations

The following figure shows the two-stage dual-supply MOSFET amplifier circuit that will be designed in this lab.



DC drain currents of  $M_1$  and  $M_4$  are set by the two current mirrors as follows:

$$I_{D1} = I_{D2} = I_{D3} = \frac{V_{SS} - V_{GS3}}{R_{B1}} = \frac{k'_n W}{2 L} (V_{GS3} - V_{tn})^2 \quad (1)$$

$$I_{D4} = I_{D5} = I_{D6} = \frac{V_{SS} - V_{GS6}}{R_{B2}} = \frac{k'_n W}{2 L} (V_{GS6} - V_{tn})^2 \quad (2)$$

For  $M_1$ ,  $M_2$  and  $M_5$ , the following should be satisfied for the active operation:

$$V_{DS} \geq V_{ov} = V_{GS} - V_{tn} \quad (3)$$

The signal swing at the drain of  $M_1$  is limited by  $V_{DD}$  and  $-V_{SS} + V_{ov2} + V_{ov1}$ , provided that the gate bias of  $M_1$  is arranged to have the maximum possible swing. However, the minimum value at  $V_{d1}$  is usually limited by  $-V_{SS} + V_{ov5} + V_{GS4}$ , which is typically higher than  $-V_{SS} + V_{ov2} + V_{ov1}$ . In order to maximize the symmetrical swing, the DC bias at  $V_{D1}$  may be centered between the upper and the lower limit. However, centering the DC bias is not always necessary, since it may conflict with other specifications. Nevertheless, the difference between  $V_{D1}$  and the upper or lower limit should be greater than the desired swing at that node.

As in the case of BJT emitter-follower, MOS source follower bias current can be determined from

$$I_{D5} \geq \frac{\text{0-to-peak output swing}}{R_L} \quad (4)$$

AC small-signal parameters can be obtained as:

$$A_v = \frac{v_{out}}{v_{in}} \approx -\frac{R_D}{\frac{1}{g_{m1}}} \frac{R_L}{R_L + \frac{1}{g_{m4}}} = -g_{m1} R_D \frac{R_L}{R_L + \frac{1}{g_{m4}}} \quad (5)$$

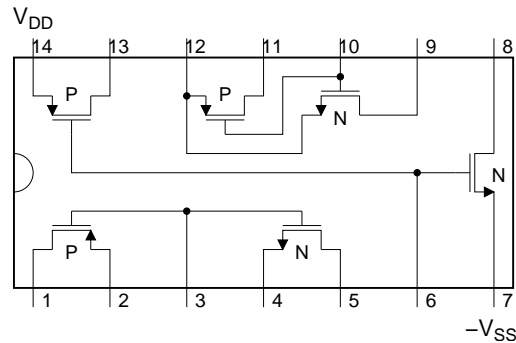
where

$$g_m = k'_n \frac{W}{L} V_{ov} = \sqrt{2k'_n \frac{W}{L} I_D} \quad (6)$$

CD4007 transistor array will be used for the implementation of the amplifier. Transistor symbols N4007 and P4007 (NMOS and PMOS, respectively) are available within the CMOS library for PSPICE. Device parameters of CD4007 are approximately given as follows:

NMOS	PMOS
$k'_n = 100 \mu A/V^2$	$k'_p = 50 \mu A/V^2$
$V_{tn} = 1.4 V$	$V_{tp} = -1.35 V$
$W = 6 \mu m$	$W = 15 \mu m$
$L = 1 \mu m$	$L = 1 \mu m$

Connection diagram of the CD4007 chip (top view) is shown below.



Note that all P-channel substrates are connected to  $V_{DD}$  and all N-channel substrates are connected to  $-V_{SS}$ .

## 2 Pre-Lab

Design a common-source MOSFET amplifier with a source follower using the following specifications:

$$\begin{aligned}
 V_{DD} = V_{SS} = 5 V & \quad R_L = 5 k\Omega & \quad \text{Operating frequency: } 5 \text{ kHz} \\
 R_{in} \geq 100 k\Omega & \quad |A_v| = 30 & \quad \text{Zero-to-peak un-clipped swing at } V_{out} \geq 2.5 V \\
 I_{supply} \leq 1.5 mA & & 
 \end{aligned}$$

1. Show all your calculations, design procedure, and final component values.
2. Verify your results using PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using PSPICE, perform Fourier analysis and determine the input and the output signal amplitudes resulting in 5% total harmonic distortion (THD) at the output. Submit transient and Fourier plots, and the distortion data from the output file.
4. Be prepared to discuss your design at the beginning of the lab period with your TA.

## 3 Lab Procedure

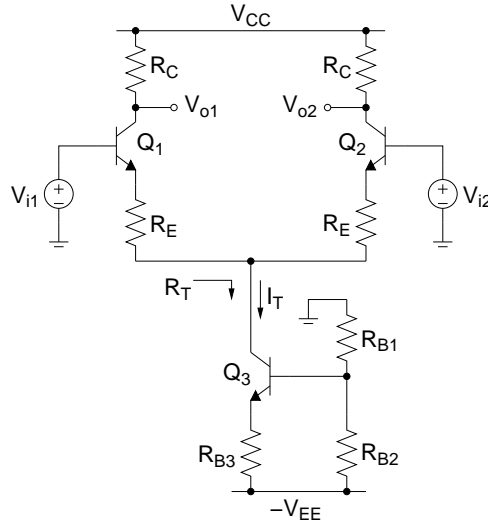
1. Construct the amplifier you designed in the pre-lab.
2. Measure  $I_{D1}$ ,  $I_{D4}$ ,  $V_{D1}$ ,  $V_{D2}$  and  $V_{D5}$ . If any DC bias value (especially  $I_D$ ) is **significantly** different than the one obtained from Pspice simulations, modify your circuit (i.e. change  $R_{B1}$ ,  $R_{B2}$ ,  $R_{G1}$ , or  $R_{G2}$ ) to get the desired DC bias before you move onto the next step.
3. Measure  $A_v$ ,  $R_{in}$ , and  $I_{supply}$  (for both  $V_{DD}$  and  $-V_{SS}$ ).
4. Measure the maximum un-clipped output signal amplitude.
5. Apply the input signal level resulting in 5% THD at the output, and measure the input and output signal amplitudes.
6. Prepare a data sheet showing your simulated and measured values.
7. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.

# ECEN 326 LAB 4

## Design of a BJT Differential Amplifier

### 1 Circuit Topology and Design Equations

The following figure shows a typical BJT differential amplifier. Assume  $\beta \geq 100$  and  $V_A = 75 V$ .



The tail current source ( $I_T$ ) can be calculated from

$$I_T \approx \frac{\frac{R_{B2}}{R_{B1} + R_{B2}} V_{EE} - 0.7}{R_{B3}}$$

provided that  $I_{B3} \ll I_{R_{B2}}$ . DC collector currents of  $Q_1$  and  $Q_2$  are

$$I_{C1} = I_{C2} \approx \frac{I_T}{2}$$

Assuming  $r_{o1}, r_{o2} \gg R_C, R_E$ , small-signal differential-mode gain can be obtained as

$$A_{dm} = \frac{v_{od}}{v_{id}} \approx -\frac{R_C}{r_{e1} + R_E}$$

where  $r_{e1} \approx V_T/I_{C1}$ . Common-mode gain can be found as

$$A_{cm} = \frac{v_{oc}}{v_{ic}} \approx -\frac{R_C}{r_{e1} + R_E + 2R_T}$$

where

$$R_T = r_{o3} + R_{BB} + g_{m3} \frac{r_{\pi 3}}{r_{\pi 3} + (R_{B1} \parallel R_{B2})} r_{o3} R_{BB}$$

$$R_{BB} = R_{B3} \parallel (r_{\pi 3} + (R_{B1} \parallel R_{B2}))$$

Common-mode rejection ratio (CMRR), differential-mode input resistance ( $R_{id}$ ) and common-mode input resistance ( $R_{ic}$ ) are given by

$$\begin{aligned} \text{CMRR} &= 20 \log \left| \frac{A_{dm}}{A_{cm}} \right| \\ R_{id} &\approx 2(\beta + 1)(R_E + r_{e1}) \\ R_{ic} &\approx (\beta + 1)(2R_T \parallel r_{o1}) \end{aligned}$$

Because of mismatches between the transistors and load resistors, a non-zero differential output voltage will result when the differential input voltage is zero. We may refer this output offset voltage back to the input as

$$V_{OS} = \frac{V_o}{A_{dm}}$$

$V_{OS}$  is known as the input-referred offset voltage. Since the two sources of the offset voltage are uncorrelated, it can be estimated as

$$V_{OS} = V_T \sqrt{\left(\frac{\Delta R_C}{R_C}\right)^2 + \left(\frac{\Delta I_S}{I_S}\right)^2}$$

## 2 Pre-Lab

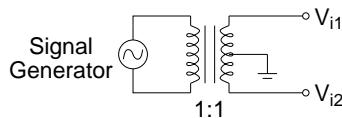
Design a BJT differential amplifier with the following specifications:

$$\begin{array}{lll} V_{ic} = 0 \text{ V} & I_{supply} \leq 3 \text{ mA} & \text{Zero-to-peak un-clipped swing at } V_{o1} \geq 2.5 \text{ V} \\ V_{CC} = V_{EE} = 5 \text{ V} & |A_{dm}| = 40 & \text{Operating frequency: 1 kHz} \\ R_{id} \geq 20 \text{ k}\Omega & \text{CMRR} \geq 70 \text{ dB} & \end{array}$$

1. Show all your calculations and final component values.
2. Verify your results using PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using PSPICE, perform Fourier analysis and determine the differential input and output signal amplitudes resulting in 1% and 5% total harmonic distortion (THD) at the differential output. Submit transient and Fourier plots, and the distortion data from the output file for both cases.
4. Be prepared to discuss your design at the beginning of the lab period with your TA.

## 3 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.
2. Connect  $V_{i1}$  and  $V_{i2}$  to ground and record all DC quiescent voltages and currents.
3. Measure  $I_{supply}$  and the output offset voltage  $V_{o1} - V_{o2}$ .
4. Using a 1:1 center-tapped transformer, apply differential input signals to the amplifier as shown below:



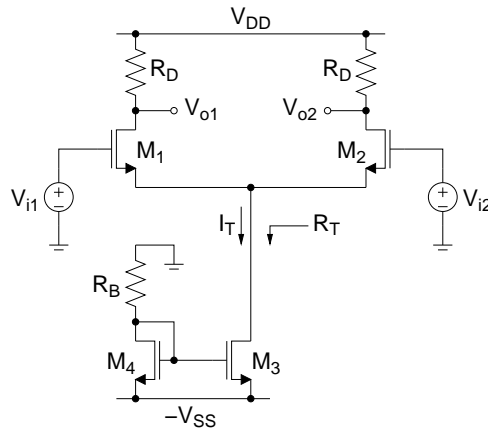
5. Measure the maximum un-clipped output signal amplitude at  $V_{o1}$ .
6. Measure  $A_{dm}$  and  $R_{id}$ .
7. Apply the input signal levels resulting in 1% and 5% THD at the differential output voltage, and measure the input and output signal amplitudes.
8. Disconnect the transformer and connect both inputs to the signal generator. Measure  $A_{cm}$  and calculate CMRR.
9. Prepare a data sheet showing your simulated and measured values.
10. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.

# ECEN 326 LAB 5

## Design of a MOS Differential Amplifier

### 1 Circuit Topology

The following figure shows a typical MOS differential amplifier. Assume  $k'_n = 100 \mu\text{A}/\text{V}^2$ ,  $V_{tn} = 1.4 \text{ V}$ ,  $\lambda_n = 0.01 \text{ V}^{-1}$ ,  $W = 6 \mu\text{m}$ , and  $L = 1 \mu\text{m}$  for all NMOS transistors.



The tail current source ( $I_T$ ) can be calculated from

$$\begin{aligned} V_{SS} &= I_{D4}R_B + V_{GS4} \\ I_{D4} &= \frac{k'_n W}{2 L} (V_{GS4} - V_{tn})^2 \\ I_T &= I_{D3} = I_{D4} \end{aligned}$$

DC drain currents of  $M_1$  and  $M_2$  are

$$I_{D1} = I_{D2} = \frac{I_T}{2}$$

Assuming  $r_{o1}, r_{o2} \gg R_D$ , small-signal differential-mode gain can be obtained as

$$A_{dm} = \frac{v_{od}}{v_{id}} \approx -\frac{R_D}{\frac{1}{g_{m1}}} = -g_{m1}R_D$$

where  $g_{m1} = \sqrt{2k'_n \frac{W}{L} I_{D1}}$ . Common-mode gain can be found as

$$A_{cm} = \frac{v_{oc}}{v_{ic}} \approx -\frac{R_D}{\frac{1}{g_{m1}} + 2R_T}$$

where  $R_T = r_{o3} = \frac{1}{\lambda_n I_{D3}}$ . Common-mode rejection ratio (CMRR) can be calculated from

$$\text{CMRR} = 20 \log \left| \frac{A_{dm}}{A_{cm}} \right|$$

## 2 Pre-Lab

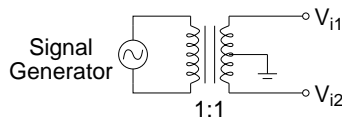
Design a MOS differential amplifier with the following specifications:

$V_{ic} = 0\text{ V}$	$I_{supply} \leq 0.5\text{ mA}$	THD $\leq 5\%$ for $V_{od} = 5\text{ V}$ 0-to-peak @ 1 kHz
$V_{DD} = V_{SS} = 5\text{ V}$	$ A_{dm}  \geq 10$	

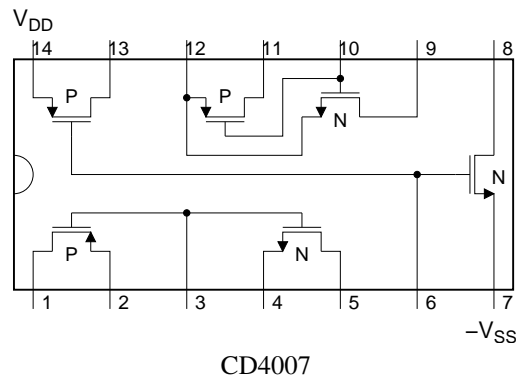
1. Show all your calculations, design procedure, and final component values.
2. Simulate your circuit using N4007 transistor models in PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using PSPICE, perform Fourier analysis and show that the total harmonic distortion (THD) is less than 5% when the differential output voltage ( $V_{od}$ ) is 5 V zero-to-peak at 1 kHz. Submit transient and Fourier plots for  $V_{od}$ , and the distortion data from the output file.
4. Be prepared to discuss your design at the beginning of the lab period with your TA.

## 3 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.
2. Connect  $V_{i1}$  and  $V_{i2}$  to ground and record all DC quiescent voltages and currents. If any DC bias value (especially  $I_D$ ) is **significantly** different than the one obtained from Pspice simulations, modify your circuit to get the desired DC bias before you move onto the next step.
3. Measure  $I_{supply}$  and the output offset voltage  $V_{o1} - V_{o2}$ .
4. Using a 1:1 center-tapped transformer, apply differential input signals at 1 kHz to the amplifier as shown below, and measure  $A_{dm}$ .



5. Adjust the input signal level so that the differential output voltage is 5 V zero-to-peak. Measure the THD at the differential output.
6. Disconnect the transformer and connect both inputs to the signal generator. Measure  $A_{cm}$  and calculate CMRR.
7. Prepare a data sheet showing your simulated and measured values.
8. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.

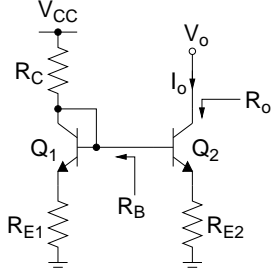


# ECEN 326 LAB 6

## Design of Current Mirrors

### 1 Circuit Topologies

#### NPN Simple Current Mirror:



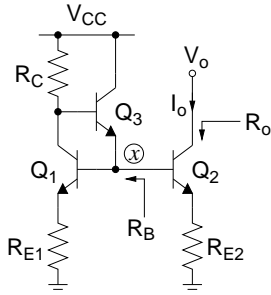
$$I_o \approx \frac{V_{CC} - 0.7}{R_C + R_{E1}} \frac{R_{E1}}{R_{E2}}, \quad V_{o,min} = V_{CE2,sat} + I_o R_{E2}$$

$$R_o = g'_{m2} r_{o2} R'_E + r_{o2} + R'_E$$

$$g'_{m2} = g_{m2} \frac{r_{\pi 2}}{r_{\pi 2} + R_B}, \quad R'_E = R_{E2} \parallel (r_{\pi 2} + R_B)$$

$$R_B = R_C \parallel (r_{e1} + R_{E1})$$

#### NPN Simple Current Mirror with $\beta$ Helper:



$$I_o \approx \frac{V_{CC} - 1.4}{R_C + R_{E1}} \frac{R_{E1}}{R_{E2}}, \quad V_{o,min} = V_{CE2,sat} + I_o R_{E2}$$

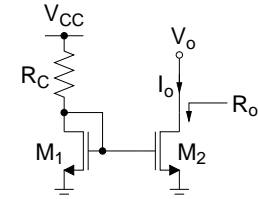
$$R_o = g'_{m2} r_{o2} R'_E + r_{o2} + R'_E$$

$$g'_{m2} = g_{m2} \frac{r_{\pi 2}}{r_{\pi 2} + R_B}, \quad R'_E = R_{E2} \parallel (r_{\pi 2} + R_B)$$

$$R_B = \left( \frac{R_C}{\beta + 1} + \frac{(\beta + 1)r_{e1}}{N} \right) \parallel \left[ \frac{r_{e1} + R_{E1}}{\beta} \left( 1 + \frac{(\beta + 1)^2 r_{e1}}{N R_C} \right) \right] \parallel (\beta + 1)(r_{e1} + R_{E1})$$

$N$  : Number of base terminals connected to the node  $\textcircled{x}$

#### NMOS Simple Current Mirror:

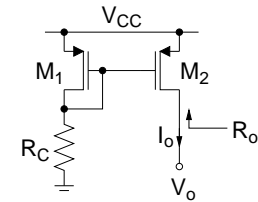


$$I_{D1} = \frac{V_{CC} - V_{GS1}}{R_C} = \frac{k'_n}{2} \left( \frac{W}{L} \right)_1 (V_{GS1} - V_{tn})^2, \quad V_{tn} < V_{GS1} < V_{CC}$$

$$I_o = \frac{(W/L)_2}{(W/L)_1} I_{D1}, \quad V_{o,min} = V_{GS1} - V_{tn} = V_{ov1}$$

$$R_o = r_{o2}$$

#### PMOS Simple Current Mirror:

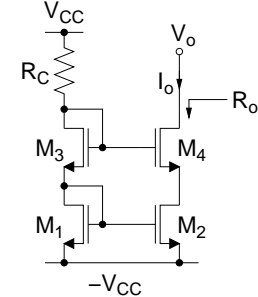


$$I_{D1} = \frac{V_{CC} - V_{SG1}}{R_C} = \frac{k'_p}{2} \left( \frac{W}{L} \right)_1 (V_{SG1} - |V_{tp}|)^2, \quad |V_{tp}| < V_{SG1} < V_{CC}$$

$$I_o = \frac{(W/L)_2}{(W/L)_1} I_{D1}, \quad V_{o,max} = V_{CC} - (V_{SG1} - |V_{tp}|) = V_{CC} - V_{ov1}$$

$$R_o = r_{o2}$$

#### NMOS Cascode Current Mirror:



$$(W/L)_1 = (W/L)_3, \quad (W/L)_2 = (W/L)_4$$

$$I_{D1} = \frac{2V_{CC} - 2V_{GS1}}{R_C} = \frac{k'_n}{2} \left( \frac{W}{L} \right)_1 (V_{GS1} - V_{tn})^2, \quad V_{tn} < V_{GS1} < \frac{V_{CC}}{2}$$

$$I_o = \frac{(W/L)_2}{(W/L)_1} I_{D1}, \quad V_{o,min} = -V_{CC} + V_{GS1} + V_{ov1} = -V_{CC} + 2V_{ov1} + V_{tn}$$

$$R_o = g_{m4} r_{o4} r_{o2} + r_{o4} + r_{o2}$$

## 2 Pre-Lab

The following table shows transistor device parameters. Use  $V_{CC} = 5V$  for all calculations.

<b>NPN</b> Q2N3904	<b>NMOS</b> N4007	<b>PMOS</b> P4007
$\beta = 140$ $V_{CE,sat} = 0.2 V$ $V_A = 75 V$	$k'_n = 100 \mu A/V^2$ $V_{tn} = 1.4 V$ $W = 6 \mu m$ $L = 1 \mu m$ $\lambda_n = 0.01 V^{-1}$	$k'_p = 50 \mu A/V^2$ $V_{tp} = -1.35 V$ $W = 15 \mu m$ $L = 1 \mu m$ $\lambda_p = 0.02 V^{-1}$

1. Calculate  $R_C$ ,  $R_o$ , and the output operating voltage range for the current mirrors in the following table:

<b>(a)</b>	NPN Simple Current Mirror	$R_{E1} = R_{E2} = 100\Omega$	$I_o = 1mA$
<b>(b)</b>	NPN Simple Current Mirror with $\beta$ Helper	$R_{E1} = R_{E2} = 100\Omega$	$I_o = 1mA$
<b>(c)</b>	NPN Simple Current Mirror with $\beta$ Helper	$R_{E1} = 100\Omega, R_{E2} = 50\Omega, Q_2 = 2 \times Q_1^\dagger$	$I_o = 2mA$
<b>(d)</b>	NMOS Simple Current Mirror	$(W/L)_1 = (W/L)_2 = 6\mu/1\mu$	$I_o = 100\mu A$
<b>(e)</b>	NMOS Simple Current Mirror	$(W/L)_1 = 6\mu/1\mu, (W/L)_2 = 12\mu/1\mu$	$I_o = 200\mu A$
<b>(f)</b>	PMOS Simple Current Mirror	$(W/L)_1 = (W/L)_2 = 15\mu/1\mu$	$I_o = 100\mu A$
<b>(g)</b>	NMOS Cascode Current Mirror	$W/L = 6\mu/1\mu$	$I_o = 100\mu A$

$^\dagger Q_2$  is composed of two transistors (each identical to  $Q_1$ ) connected in parallel.

2. For each current mirror, perform DC simulation by sweeping  $V_o$  from 0 to  $V_{CC}$  (for the cascode mirror, from  $-V_{CC}$  to  $V_{CC}$ ), and plot the output current  $I_o$ .
3. For each current mirror, perform AC simulation while  $V_{o,dc} = 2V$ , and plot the output resistance  $R_o$ .
4. Submit all simulation plots and the circuit schematics with DC bias points annotated (@  $V_o = 2V$ ).
5. Be prepared to discuss your designs at the beginning of the lab period with your TA.

## 3 Lab Procedure

1. Construct all current mirrors you designed in the pre-lab.
2. For each circuit, measure  $I_o$ ,  $R_o$  and the output operating voltage range.
3. Prepare a data sheet showing your simulated and measured values.
4. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.



# ECEN 326 LAB 7

## Design of a BJT Operational Transconductance Amplifier

### 1 Circuit Topology

The operational transconductance amplifier (OTA) schematic that will be designed in this lab is shown in Fig. 1.

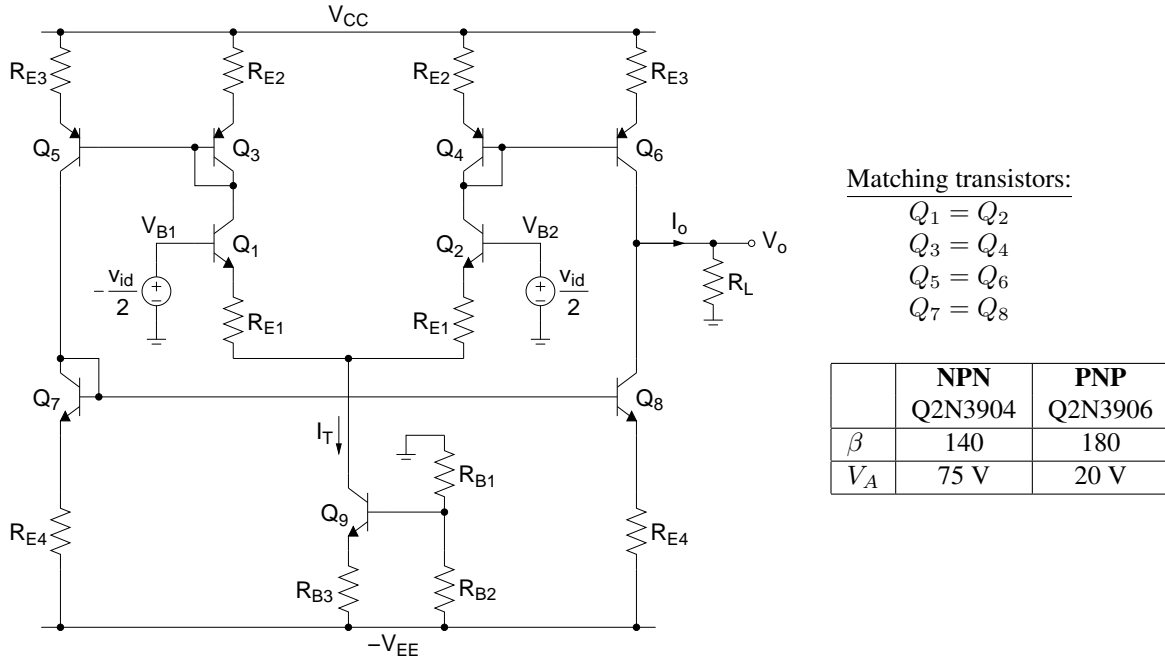


Figure 1: Operational transconductance amplifier (OTA) schematic.

#### DC Biasing and Large-Signal Analysis:

Assuming  $I_{B9} \ll I_{R_{B2}}$ , the tail current source ( $I_T$ ) can be calculated from

$$I_T \approx \frac{\frac{R_{B2}}{R_{B1} + R_{B2}} V_{EE} - 0.7}{R_{B3}} \quad (1)$$

Collector currents of  $Q_1 - Q_4$  for  $V_{id} = 0$  can be found as

$$I_{C1-C4} \approx \frac{I_T}{2} \quad (2)$$

If the ratio of  $I_5$  to  $I_3$  is less than an order of magnitude, then  $V_{EB5} \approx V_{EB3}$ , therefore,

$$I_{C5} R_{E3} = I_{C3} R_{E2} \Rightarrow \frac{I_{C5}}{I_{C3}} \approx \frac{R_{E2}}{R_{E3}} \quad (3)$$

An OTA is commonly used in the open-loop configuration. For proper operation, the maximum differential input amplitude  $|v_{id,max}|$  needs to be determined. With emitter degeneration resistors  $R_{E1}$ ,  $|v_{id,max}|$  can be approximately found as

$$|v_{id,max}| = I_T R_{E1} \quad (4)$$

A more accurate limit can be defined by a maximum distortion specification. It is also necessary to determine what range of common-mode input voltages will allow all transistors in the input stage to remain in the active region. Defining the minimum collector-emitter voltage for the active operation as  $V_{CE,sat}$ , the range of  $V_{CM}$  can be approximately given by

$$V_{CC} - I_T R_{E2} - V_{CE,sat} > V_{CM} > -V_{EE} + I_T R_{B3} + V_{CE,sat} + I_T R_{E1} + V_{BE,on} \quad (5)$$

### AC Small-Signal Analysis:

Since the circuit is not symmetrical, half-circuit concepts will not be useful. Figure 2 shows the AC small-signal equivalent circuit to determine the equivalent transconductance

$$G_m = \frac{-i_{sc}}{v_{id}} \quad (6)$$

where the output resistances ( $r_o$ ) of transistors are assumed to be infinite.

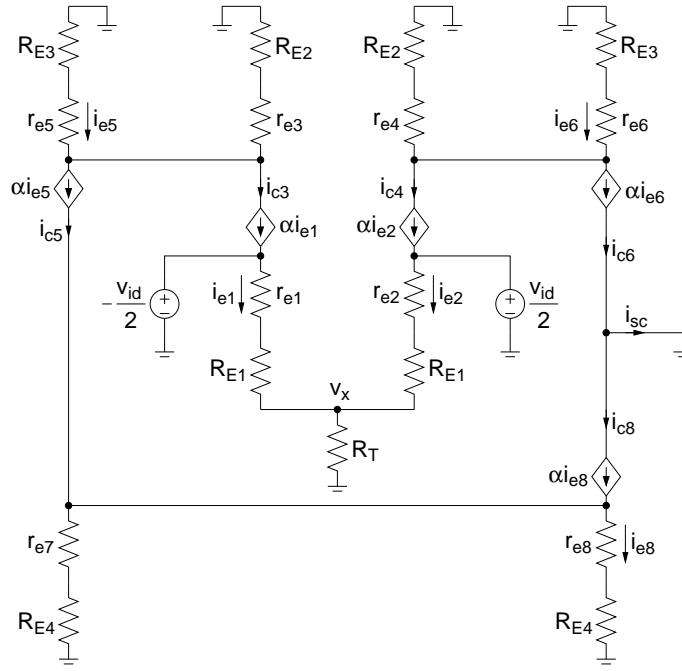


Figure 2: Small-signal circuit of the OTA.

KCL at  $v_x$  yields

$$\frac{v_x}{R_T} + \frac{v_x - \left(-\frac{v_{id}}{2}\right)}{r_{e1} + R_{E1}} + \frac{v_x - \left(\frac{v_{id}}{2}\right)}{r_{e2} + R_{E1}} = 0 \quad (7)$$

Since  $Q_1$  and  $Q_2$  are identical,  $r_{e1} = r_{e2}$ , resulting in

$$\frac{v_x}{R_T} + \frac{v_x}{r_{e1} + R_{E1}} + \frac{v_x}{r_{e2} + R_{E1}} = 0 \Rightarrow v_x = 0 \quad (8)$$

Therefore,  $v_x$  is a virtual AC ground for differential input signals. The collector current of  $Q_6$  can be found as follows:

$$i_{c4} = \alpha i_{e2} \approx \frac{v_{id}/2}{R_{E1} + r_{e2}} \quad (9)$$

$$i_{c6} \approx \frac{i_{c4}(R_{E2} + r_{e4})}{R_{E3} + r_{e6}} = \frac{v_{id}}{2} \frac{1}{R_{E1} + r_{e2}} \frac{R_{E2} + r_{e4}}{R_{E3} + r_{e6}} \quad (10)$$

Similarly,  $i_{c5}$  and  $i_{c8}$  can be found as

$$i_{c5} \approx -\frac{v_{id}}{2} \frac{1}{R_{E1} + r_{e1}} \frac{R_{E2} + r_{e3}}{R_{E3} + r_{e5}} \quad (11)$$

$$i_{c8} \approx i_{c5} \frac{R_{E4} + r_{e7}}{R_{E4} + r_{e8}} \quad (12)$$

Since  $Q_7$  and  $Q_8$  are identical,  $r_{e7} = r_{e8}$ , which yields

$$i_{c8} \approx -\frac{v_{id}}{2} \frac{1}{R_{E1} + r_{e1}} \frac{R_{E2} + r_{e3}}{R_{E3} + r_{e5}} \quad (13)$$

The short-circuit output current ( $i_{sc}$ ) can be determined as

$$i_{sc} = i_{c6} - i_{c8} = \frac{v_{id}}{2} \frac{1}{R_{E1} + r_{e2}} \frac{R_{E2} + r_{e4}}{R_{E3} + r_{e6}} - \left( -\frac{v_{id}}{2} \frac{1}{R_{E1} + r_{e1}} \frac{R_{E2} + r_{e3}}{R_{E3} + r_{e5}} \right) \quad (14)$$

Using the matching data,  $r_{e2} = r_{e1}$ ,  $r_{e4} = r_{e3}$ ,  $r_{e6} = r_{e5}$ ,

$$i_{sc} = v_{id} \frac{1}{R_{E1} + r_{e2}} \frac{R_{E2} + r_{e4}}{R_{E3} + r_{e6}} \quad (15)$$

$$(16)$$

$$G_m = -\frac{1}{R_{E1} + r_{e2}} \frac{R_{E2} + r_{e4}}{R_{E3} + r_{e6}} \quad (17)$$

The differential input resistance can be found as

$$R_{id} = 2(\beta + 1)(r_{e2} + R_{E1})$$

The output resistance can be expressed as

$$R_o \approx (g'_{m6} r_{o6} R'_{E3} + r_{o6}) \parallel (g'_{m8} r_{o8} R'_{E4} + r_{o8}) \quad (18)$$

$$g'_{m6} = g_{m6} \frac{r_{\pi 6}}{r_{\pi 6} + r_{e4} + R_{E2}}, \quad R'_{E3} = R_{E3} \parallel (r_{\pi 6} + r_{e4} + R_{E2}) \quad (19)$$

$$g'_{m8} = g_{m8} \frac{r_{\pi 8}}{r_{\pi 8} + r_{e7} + R_{E4}}, \quad R'_{E4} = R_{E4} \parallel (r_{\pi 8} + r_{e7} + R_{E4}) \quad (20)$$

We may construct an equivalent small-signal model for the OTA as shown in Fig. 3.

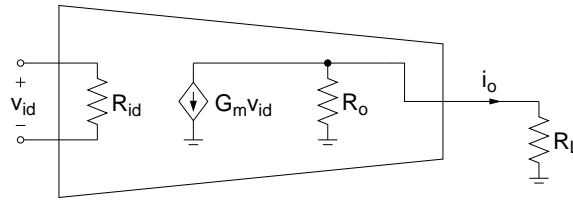


Figure 3: Equivalent small-signal model of the OTA.

## 2 Pre-Lab

Design an OTA with the following specifications:

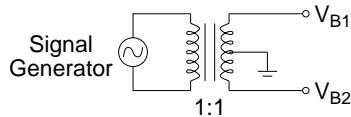
$$\begin{aligned} V_{CC} = V_{EE} = 5V & \quad G_m = 1mA/V & \quad \text{Operating frequency: } 1\text{ kHz} \\ |v_{id,max}| \geq 2V & \quad V_{CM,max} - V_{CM,min} \geq 4V & \quad I_{supply} \leq 5mA \end{aligned}$$

1. Show all your calculations and final component values.

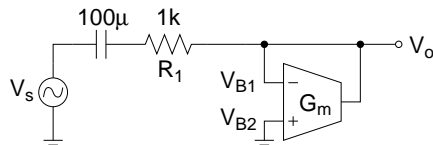
- Calculate  $R_{id}$  and  $R_o$  for your design.
- Verify your results using PSPICE (use Q2N3904 and Q2N3906 transistors). Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
- Be prepared to discuss your design at the beginning of the lab period with your TA.

### 3 Lab Procedure

- Construct the OTA you designed in the pre-lab.
- Set  $V_{id} = 0$  and record all DC quiescent voltages and currents.
- Measure  $I_{supply}$  and the short-circuit output current while  $V_{id} = 0$ .
- Using a 1:1 center-tapped transformer, apply differential input signals to the amplifier as shown below:

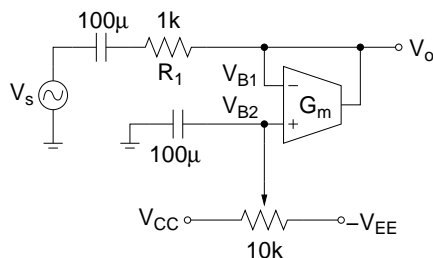


- Connect a  $1k\Omega$  resistor between the output node and ground. Using the XY mode of the scope, monitor  $V_o$  vs.  $V_{B1}$ . Measure the slope and calculate the resulting  $G_m$ .
- Increase the input amplitude until nonlinearity occurs. Measure and record the width of the input linear range ( $|v_{id,max}|$ ).
- Disconnect the transformer, ground  $V_{B2}$  and the output node, and measure the differential input resistance  $R_{id}$  at  $V_{B1}$ .
- Using the circuit setup below, measure and record the transconductance ( $G_m$ ) of your OTA.



$$\frac{V_o}{V_s} = \frac{1/G_m}{R_1 + (1/G_m)}$$

- Connect the OTA as shown in the figure below and set the amplitude of  $V_s$  to  $|v_{id,max}|$ . Using the XY mode of the scope, monitor  $V_o$  vs.  $V_s$ . Vary the potentiometer in both directions until nonlinearity occurs. Measure and record the DC voltage at  $V_{B2}$  at the two settings of the potentiometer where distortion occurs. Record these two measurements as  $V_{CM,max}$  and  $V_{CM,min}$ .



$$\frac{V_o}{V_s} = \frac{1/G_m}{R_1 + (1/G_m)}$$

- Prepare a data sheet showing your simulated and measured values.
- Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.

# ECEN 326 LAB 8

## Frequency Response of a Common-Emitter BJT Amplifier

### 1 Circuit Topology

Circuit schematic of the common-emitter amplifier is shown in Fig. 1. Capacitors  $C_B$  and  $C_C$  are used for AC coupling, whereas  $C_E$  is an AC bypass capacitor used to establish an AC ground at the emitter of  $Q_1$ .  $C_F$  is a small capacitance that will be used to control the higher 3-dB frequency of the amplifier.

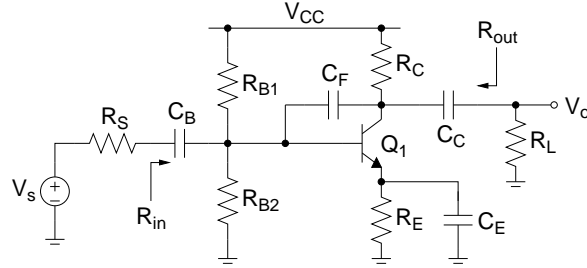


Figure 1: Common-emitter BJT amplifier.

#### 1.1 DC Biasing and Mid-band Frequency Response

For this section, assume that  $C_B = C_C = C_E = \infty$  and  $C_F = C_\pi = C_\mu = 0$ . You can find the DC collector current ( $I_C$ ) and the resistor values following the analysis provided in Lab #1. Since the topology and the requirements are slightly different, you need to make minor modifications to the design procedure and equations.

#### 1.2 Low Frequency Response

Figure 2 shows the low-frequency small-signal equivalent circuit of the amplifier. Note that  $C_F$  is ignored since its impedance at these frequencies is very high.

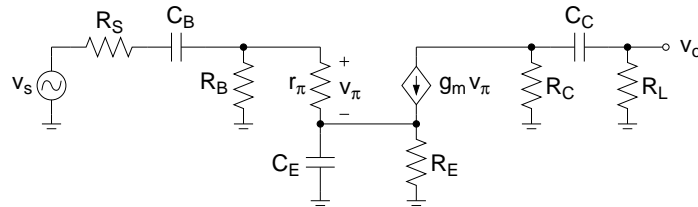


Figure 2: Low-frequency equivalent circuit.

Using short-circuit time constant analysis, the lower 3-dB frequency ( $\omega_L$ ) can be found as

$$\omega_L \approx \frac{1}{R_{1s}C_B} + \frac{1}{R_{2s}C_E} + \frac{1}{R_{3s}C_C} \quad (1)$$

where

$$R_{1s} = R_S + (R_B \parallel r_\pi) \quad (2)$$

$$R_{2s} = R_E \parallel \left( \frac{r_\pi + (R_B \parallel R_S)}{\beta + 1} \right) \quad (3)$$

$$R_{3s} = R_C + R_L \quad (4)$$

### 1.3 High Frequency Response

At high frequencies,  $C_B$ ,  $C_C$  and  $C_E$  can be replaced with a short circuit since their impedances become very small. Figure 3 shows the high-frequency small-signal equivalent circuit of the amplifier.

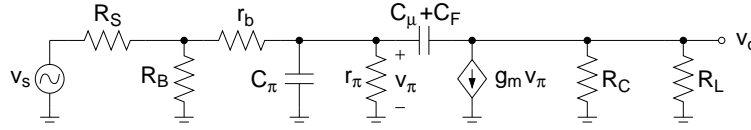


Figure 3: High-frequency equivalent circuit.

The higher 3-dB frequency ( $\omega_H$ ) can be derived as

$$\omega_H = \frac{1}{R_T \left[ C_\pi + (C_\mu + C_F) \left( 1 + g_m R_{CL} + \frac{R_{CL}}{R_T} \right) \right]} \quad (5)$$

where

$$R_T = r_\pi \parallel (r_b + (R_S \parallel R_B)) \quad (6)$$

$$R_{CL} = R_C \parallel R_L \quad (7)$$

Thus, if we assume that the common-emitter amplifier is properly characterized by these dominant low and high frequency poles, then the frequency response of the amplifier can be approximated by

$$\frac{v_o}{v_s}(s) = A_v \frac{s}{s + \omega_L} \frac{1}{1 + \frac{s}{\omega_H}} \quad (8)$$

## 2 Pre-Lab

Assuming  $C_B = C_C = C_E = \infty$  and  $C_F = C_\pi = C_\mu = 0$ , and using a Q2N2222 BJT, design a common-emitter amplifier with the following specifications:

$$\begin{aligned} V_{CC} &= 5 \text{ V} & R_S &= 50 \Omega & R_L &= 1 \text{ k}\Omega \\ R_{in} &\geq 250 \Omega & I_{supply} &\leq 8 \text{ mA} & |A_v| &\geq 50 & \text{0-to-peak unclipped output swing} &\geq 1.5 \text{ V} \end{aligned}$$

1. Show all your calculations, design procedure, and final component values.
2. Verify your results using PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using PSPICE, find the higher 3-dB frequency ( $f_H$ ) while  $C_F = 0$ .
4. Determine  $C_\pi$ ,  $C_\mu$  and  $r_b$  of the transistor from the PSPICE output file (in Probe, choose View  $\rightarrow$  Output File, scroll down to the section OPERATING POINT INFORMATION,  $C_\pi$ ,  $C_\mu$  and  $r_b$  are listed as CBE, CBC and RX, respectively). Calculate  $f_H$  using Eq. (5) and compare it with the simulation result obtained in Step 3.
5. Calculate the value of  $C_F$  to have  $f_H = 20$  kHz. Simulate the circuit to verify your result, and adjust the value of  $C_F$  if necessary.
6. Calculate  $C_B$ ,  $C_C$ ,  $C_E$  to have  $f_L = 500$  Hz. Simulate the circuit to verify your result, and adjust the values of capacitors if necessary.
7. Be prepared to discuss your design at the beginning of the lab period with your TA.

### 3 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.
2. Measure  $I_C$ ,  $V_E$ ,  $V_C$  and  $V_B$ . If any DC bias value is significantly different than the one obtained from Pspice simulations, modify your circuit to get the desired DC bias before you move onto the next step.
3. Measure  $I_{supply}$ .
4. Obtain the magnitude of the frequency response of the amplifier and determine the lower and higher 3-dB frequencies  $f_L$  and  $f_H$ .
5. At midband frequencies, measure  $A_v$ ,  $R_{in}$ , and  $R_{out}$ .
6. Measure the maximum un-clipped output signal amplitude.
7. Prepare a data sheet showing your simulated and measured values.
8. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.

# ECEN 326 LAB 9

## Frequency Response of a Cascode BJT Amplifier

### 1 Circuit Topology

Circuit schematic of the cascode amplifier is shown in Fig. 1. Capacitors  $C_B$  and  $C_C$  are used for AC coupling, whereas  $C_D$  and  $C_E$  are AC bypass capacitors.  $C_F$  is a small capacitance that will be used to control the higher 3-dB frequency of the amplifier.

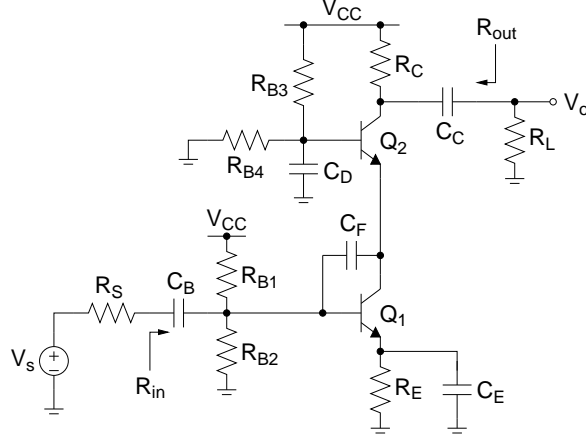


Figure 1: Cascode BJT amplifier.

#### 1.1 DC Biasing and Mid-band Frequency Response

For this section, assume that  $C_B = C_C = C_D = C_E = \infty$  and  $C_F = C_\pi = C_\mu = 0$ . You can find the DC collector currents ( $I_{C1}$  and  $I_{C2}$ ) and the resistor values following the analysis provided in Lab #2. Since the topology and the requirements are slightly different, you need to make minor modifications to the design procedure and equations.

#### 1.2 Low Frequency Response

Using short-circuit time constant analysis, the lower 3-dB frequency ( $\omega_L$ ) can be found as

$$\omega_L \approx \frac{1}{R_{1s}C_B} + \frac{1}{R_{2s}C_E} + \frac{1}{R_{3s}C_D} + \frac{1}{R_{4s}C_C} \quad (1)$$

where

$$R_{1s} = R_S + (R_{B1} \parallel R_{B2} \parallel r_{\pi 1}) \quad (2)$$

$$R_{2s} = R_E \parallel \left( r_{e1} + \frac{R_{B1} \parallel R_{B2} \parallel R_S}{\beta + 1} \right) \quad (3)$$

$$R_{3s} = R_{B3} \parallel R_{B4} \quad (4)$$

$$R_{4s} = R_C + R_L \quad (5)$$



### 1.3 High Frequency Response

The higher 3-dB frequency ( $\omega_H$ ) can be estimated using open-circuit time constant analysis

$$\omega_H \approx \frac{1}{R_{1o}C_{\pi 1} + R_{2o}(C_{\mu 1} + C_F) + R_{3o}C_{\pi 2} + R_{4o}C_{\mu 2}} \quad (6)$$

where

$$R_{1o} = r_{\pi 1} \parallel (r_{b1} + (R_{B1} \parallel R_{B2} \parallel R_S)) \quad (7)$$

$$R_{2o} = R_{1o} + r_{e2} + g_{m1}R_{1o}r_{e2} \quad (8)$$

$$R_{3o} = r_{\pi 2} \parallel \frac{1}{g_{m2}} \quad (9)$$

$$R_{4o} = R_C \parallel R_L \quad (10)$$

Thus, if we assume that the cascode amplifier is properly characterized by these dominant low and high frequency poles, then the frequency response of the amplifier can be approximated by

$$\frac{v_o}{v_s}(s) = A_v \frac{s}{s + \omega_L} \frac{1}{1 + \frac{s}{\omega_H}}$$

## 2 Pre-Lab

Assuming  $C_B = C_C = C_D = C_E = \infty$  and  $C_F = C_{\pi} = C_{\mu} = 0$ , and using Q2N2222 BJTs, design a cascode amplifier with the following specifications:

$$\begin{aligned} V_{CC} = 5 \text{ V} \quad R_S = 50 \Omega \quad R_L = 1 \text{ k}\Omega \\ R_{in} \geq 250 \Omega \quad I_{supply} \leq 8 \text{ mA} \quad |A_v| \geq 50 \quad \text{0-to-peak unclipped output swing} \geq 1.5 \text{ V} \end{aligned}$$

1. Show all your calculations, design procedure, and final component values.
2. Verify your results using PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using PSPICE, find the higher 3-dB frequency ( $f_H$ ) while  $C_F = 0$ .
4. Determine  $C_{\pi}$ ,  $C_{\mu}$  and  $r_b$  for both transistors from the PSPICE output file (in Probe, choose View  $\rightarrow$  Output File, scroll down to the section OPERATING POINT INFORMATION,  $C_{\pi}$ ,  $C_{\mu}$  and  $r_b$  are listed as CBE, CBC and RX, respectively). Calculate  $f_H$  using Eq. (6) and compare it with the simulation result obtained in Step 3.
5. Calculate the value of  $C_F$  to have  $f_H = 20$  kHz. Simulate the circuit to verify your result, and adjust the value of  $C_F$  if necessary.
6. Calculate  $C_B$ ,  $C_C$ ,  $C_D$  and  $C_E$  to have  $f_L = 500$  Hz. Simulate the circuit to verify your result, and adjust the values of capacitors if necessary.
7. Compare the value of  $f_H$  for  $C_F = 0$  with that of the common-emitter amplifier designed in the previous lab. Also compare the values of  $C_F$  required to obtain  $f_H = 20$  kHz. Comment on the differences.
8. Be prepared to discuss your design at the beginning of the lab period with your TA.

### 3 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.
2. Measure  $I_C$ ,  $V_C$ ,  $V_B$  and  $V_E$  for both transistors. If any DC bias value is significantly different than the one obtained from Pspice simulations, modify your circuit to get the desired DC bias before you move onto the next step.
3. Measure  $I_{supply}$ .
4. Obtain the magnitude of the frequency response of the amplifier and determine the lower and higher 3-dB frequencies  $f_L$  and  $f_H$ .
5. At midband frequencies, measure  $A_v$ ,  $R_{in}$ , and  $R_{out}$ .
6. Measure the maximum un-clipped output signal amplitude.
7. Prepare a data sheet showing your simulated and measured values.
8. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.

# ECEN 326 LAB 10

## Design of a BJT Shunt-Series Feedback Amplifier

### 1 Circuit Topology

Circuit schematic of the feedback amplifier to be designed in this lab is shown in Fig. 1.

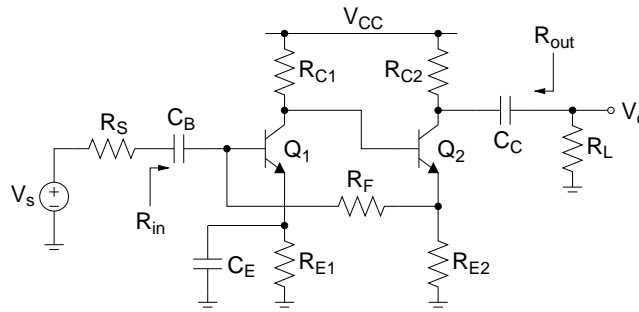


Figure 1: Feedback amplifier.

#### 1.1 DC Biasing

First, the emitter DC bias voltage of  $Q_1$  ( $V_{E1}$ ) needs to be determined. Since only  $I_{B1}$  flows through the resistor  $R_F$ , the DC voltage drop on  $R_F$  can be assumed to be negligible. Thus,  $V_{E2}$  and  $V_{C1}$  can be expressed as

$$V_{E2} \approx V_{E1} + 0.7 \quad (1)$$

$$V_{C1} \approx V_{E1} + 1.4 \quad (2)$$

To maximize the voltage swing at the output, load-line analysis is needed for the second stage. The DC equation including  $I_{C2}$  and  $V_{CE2}$  can be written as

$$V_{CC} \approx R_{C2}I_{C2} + V_{CE2} + V_{E2} \quad (3)$$

Figure 2 shows the AC load line to obtain the maximum output swing.

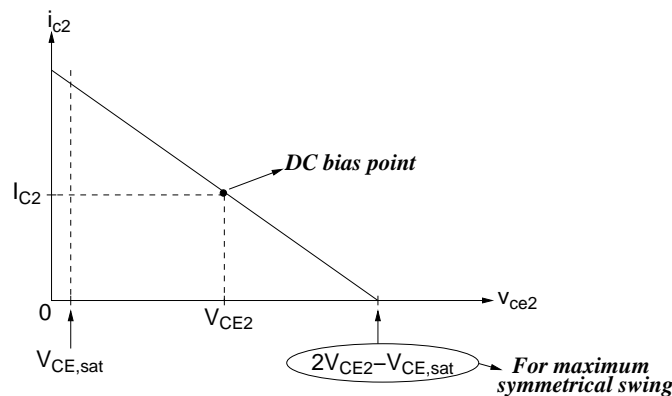


Figure 2: AC load line.

From the AC equivalent of Fig. 1, slope of the AC load line can be determined as

$$\frac{\Delta i_{c2}}{\Delta v_{ce2}} = -\frac{1}{(R_{C2} \parallel R_L) + R_{E2}} \quad (4)$$

Using the slope and the DC bias point  $(i_{c2}, v_{ce2}) = (I_{C2}, V_{CE2})$ , the load line equation can be obtained as

$$\frac{i_{c2} - I_{C2}}{v_{ce2} - V_{CE2}} = -\frac{1}{(R_{C2} \parallel R_L) + R_{E2}} \quad (5)$$

Evaluating Eq. (5) at the point  $(i_{c2}, v_{ce2}) = (0, 2V_{CE2} - V_{CE,sat})$ ,

$$I_{C2}((R_{C2} \parallel R_L) + R_{E2}) = V_{CE2} - V_{CE,sat} \quad (6)$$

Solving Eqs. (3) and (6), the optimum  $I_{C2}$  to obtain the maximum symmetrical swing can be found as

$$I_{C2} = \frac{V_{CC} - 2V_{E2} - V_{CE,sat}}{R_{C2} + (R_{C2} \parallel R_L)} \quad (7)$$

After determining  $I_{C2}$ , 0-to-peak voltage swing at the output can be calculated as

$$V_{sw} = I_{C2}(R_{C2} \parallel R_L) = \frac{V_{CC} - 2V_{E2} - V_{CE,sat}}{1 + \frac{R_{C2}}{R_{C2} \parallel R_L}} = \frac{V_{CC} - 2V_{E2} - V_{CE,sat}}{2 + \frac{R_{C2}}{R_L}} \quad (8)$$

Since  $V_{E1}$  and  $V_{C1}$  are already determined,  $I_{C1}$  can be chosen based on other specifications. The remaining components can be calculated as

$$R_{E1} = \frac{V_{E1}}{I_{C1}} \quad (9)$$

$$R_{C1} = \frac{V_{CC} - V_{C1}}{I_{C1}} \quad (10)$$

$$R_{E2} = \frac{V_{E2}}{I_{C2}} \quad (11)$$

## 1.2 Feedback Analysis and Mid-band Frequency Response

AC equivalent of the amplifier in the mid-band frequency range is shown in Fig. 3.

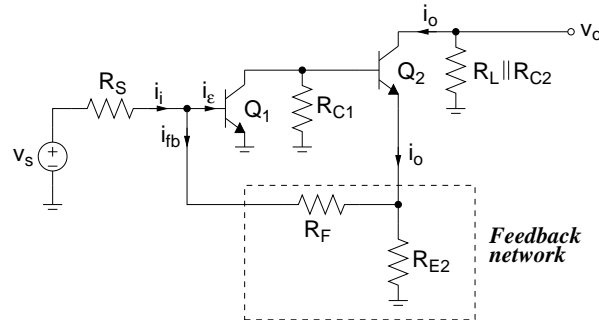


Figure 3: AC equivalent circuit.

The input port of the feedback network in Fig. 3 is not directly connected to the output node ( $v_o$ ). Therefore, the sampled output signal is not a voltage. Defining the output current as

$$i_o = -\frac{v_o}{R_L \parallel R_{C2}} \quad (12)$$

it can be concluded that  $i_o$  is sampled by the feedback network. At the amplifier's input, subtraction of the feedback signal is performed in the current domain,

$$i_i - i_{fb} = i_e \quad (13)$$

Therefore, the type of feedback is shunt-series. The next step is to obtain the  $g$  parameters of the feedback network as shown in Fig. 4.

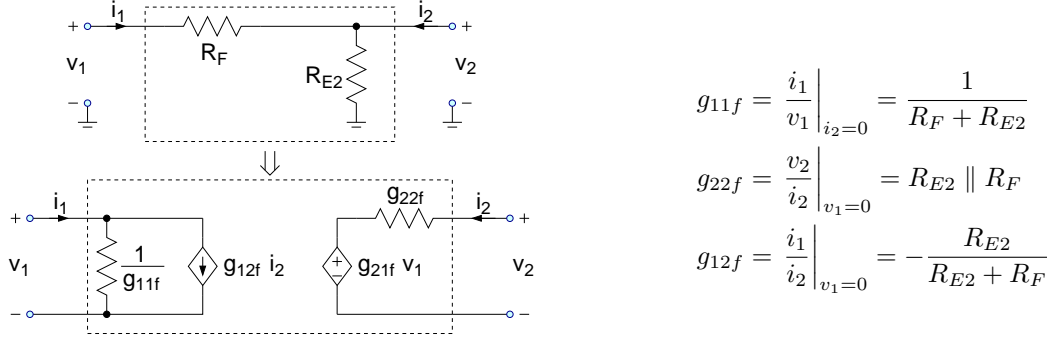


Figure 4: Calculation of the  $g$ -parameters of the feedback network.

Replacing the feedback network with its two-port equivalent and converting the input source into current, the amplifier circuit can be arranged as in Fig. 5.

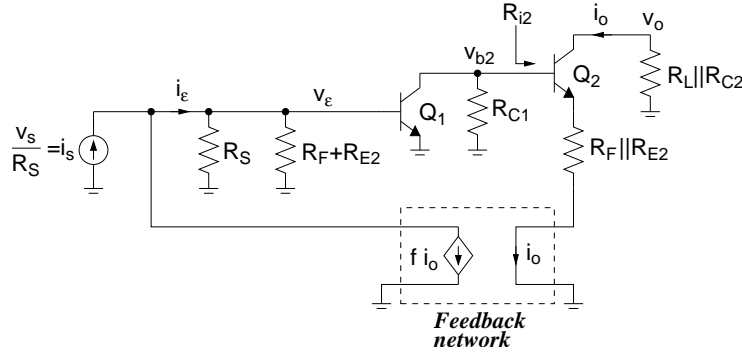


Figure 5: Amplifier with the ideal feedback network.

From Fig. 5, assuming  $r_{o1}$  and  $r_{o2}$  are large, the parameters  $a$  and  $f$  can be obtained as follows

$$v_\varepsilon = i_\varepsilon (R_S \parallel (R_F + R_{E2}) \parallel r_{\pi 1}) \quad (14)$$

$$\frac{v_{b2}}{v_\varepsilon} = -\frac{R_{C1} \parallel R_{i2}}{r_{e1}} \quad (15)$$

$$R_{i2} = (\beta + 1)(r_{e2} + (R_F \parallel R_{E2})) \quad (16)$$

$$\frac{v_o}{v_{b2}} = -\frac{R_L \parallel R_{C2}}{r_{e2} + (R_F \parallel R_{E2})} \quad (17)$$

$$v_o = -i_o (R_L \parallel R_{C2}) \quad (18)$$

$$a = \frac{i_o}{i_\varepsilon} = -\frac{(R_S \parallel (R_F + R_{E2}) \parallel r_{\pi 1})(R_{C1} \parallel R_{i2})}{r_{e1}(r_{e2} + (R_F \parallel R_{E2}))} \quad (19)$$

$$f = g_{12f} = -\frac{R_{E2}}{R_{E2} + R_F} \quad (20)$$

The current-mode close-loop amplifier parameters are

$$A_i = \frac{i_o}{i_s} = \frac{a}{1 + af} \quad (21)$$

$$Z_i = \frac{z_i}{1 + af} \quad (22)$$

$$Z_o = (1 + af)z_o \quad (23)$$

where

$$z_i = R_S \parallel (R_F + R_{E2}) \parallel r_{\pi 1} \quad (24)$$

$$z_o = R_T + r_{o2} + g_{m2} \frac{r_{\pi 2}}{r_{\pi 2} + (r_{o1} \parallel R_{C1})} r_{o2} R_T \quad (25)$$

$$R_T = R_F \parallel R_{E2} \parallel [r_{\pi 2} + (r_{o1} \parallel R_{C1})] \quad (26)$$

Figure 6 shows the current-mode equivalent model of the amplifier.

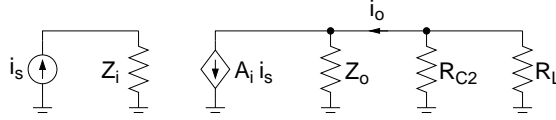


Figure 6: Current-mode equivalent model of the amplifier.

As the final step, the current-mode model needs to be converted to a voltage-mode amplifier. Figure 7 shows the equivalent amplifier where  $R_S$  is separated from  $Z_i$  and the controlled source depends on  $i_{in}$ .

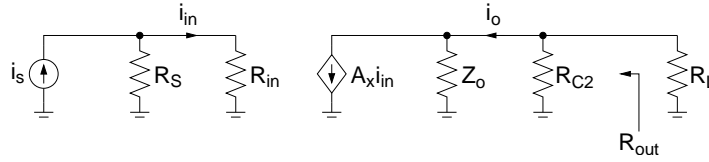


Figure 7: Current-mode amplifier with  $R_S$  separated.

$R_{in}$  and  $A_x$  in Fig. 7 can be found as follows

$$Z_i = R_S \parallel R_{in} = \frac{1}{\frac{1}{R_S} + \frac{1}{R_{in}}} \Rightarrow R_{in} = \frac{1}{\frac{1}{Z_i} - \frac{1}{R_S}} \quad (27)$$

$$i_{in} = \frac{R_S}{R_S + R_{in}} i_s \Rightarrow A_x = A_i \left( 1 + \frac{R_{in}}{R_S} \right) \quad (28)$$

Voltage-mode equivalent model of the amplifier can be obtained after final conversion as shown in Fig. 8.

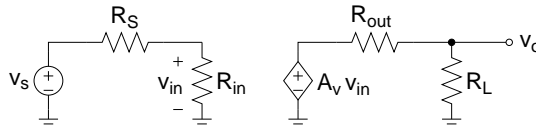


Figure 8: Voltage-mode equivalent model of the amplifier.

$R_{out}$  and  $A_v$  in Fig. 8 can be found as follows

$$R_{out} = Z_o \parallel R_{C2} \approx R_{C2} \quad (29)$$

$$A_v = -A_x \frac{R_{out}}{R_{in}} = -A_i \left( 1 + \frac{R_{in}}{R_S} \right) \frac{R_{out}}{R_{in}} \quad (30)$$

Finally, the voltage gain  $v_o/v_s$  can be calculated as

$$\frac{v_o}{v_s} = \frac{R_{in}}{R_S + R_{in}} A_v \frac{R_L}{R_{out} + R_L} \quad (31)$$

## 2 Pre-Lab

Using Q2N2222 transistors, design the feedback amplifier with the following specifications:

$$\begin{array}{llll} V_{CC} = 10\text{ V} & R_S = 50\Omega & R_L = 10\text{ k}\Omega & V_{E1} \geq 0.4\text{ V} \\ af \geq 5 & I_{supply} \leq 10\text{ mA} & |v_o/v_s| \geq 80 & \text{0-to-peak unclipped output swing} \geq 3.5\text{ V} \end{array}$$

1. Show all your calculations, design procedure, and final component values.
2. Using PSPICE, find  $a$ ,  $f$ ,  $I_{supply}$ ,  $R_{in}$ ,  $R_{out}$  and  $v_o/v_s$  to verify your results. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using PSPICE, perform Fourier analysis to determine the THD of 3.5 V (0-to-peak) output waveform at 1 kHz. Submit transient and Fourier plots, and the distortion data from the output file.
4. Be prepared to discuss your design at the beginning of the lab period with your TA.

## 3 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.
2. Measure  $I_C$ ,  $V_C$ ,  $V_B$  and  $V_E$  for both transistors. If any DC bias value is significantly different than the one obtained from Pspice simulations, modify your circuit to get the desired DC bias before you move onto the next step.
3. Measure  $I_{supply}$ .
4. At midband frequencies, measure  $v_o/v_s$ ,  $R_{in}$  and  $R_{out}$ .
5. Measure the maximum un-clipped output signal amplitude.
6. Measure the THD when the output is 3.5 V (0-to-peak) sinewave at 1 kHz.
7. Prepare a data sheet showing your simulated and measured values.
8. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.

# ECEN 326 LAB 11

## Design of a Two-Stage Amplifier with Miller Compensation

### 1 Circuit Topology

Figure 1 shows the two-stage differential amplifier to be designed in this lab.  $C_L$  represents the load capacitor, whereas  $C_M$  is the Miller compensation capacitor.

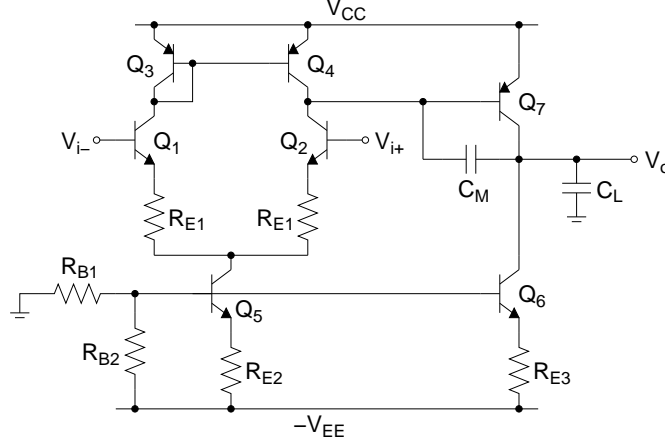


Figure 1: Two-stage differential amplifier.

Defining  $V_i = (V_{i+} - V_{i-})$ , the transfer function can be obtained as

$$\frac{V_o}{V_i}(s) = a(s) \approx \frac{a_o}{\left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right)} \quad (1)$$

where

$$a_o \approx g'_{m2} R_{o1} g_{m7} R_{o2} \quad (2)$$

$$g'_{m2} \approx \frac{g_{m2}}{1 + g_{m2} R_{E1}} \quad (3)$$

$$R_{o1} \approx r_{\pi 7} \parallel r_{o4} \parallel (r_{o2} + g_{m2} r_{o2} R_{E1}) \quad (4)$$

$$R_{o2} \approx r_{o7} \parallel (g_{m6} r_{o6} (R_{E3} \parallel r_{\pi 6}) + r_{o6}) \quad (5)$$

$$p_1 \approx -\frac{1}{g_{m7} R_{o1} R_{o2} C_M} \quad (6)$$

$$p_2 \approx -\frac{g_{m7}}{C_L} \quad (7)$$

Assuming  $|p_2| \gg |p_1|$  and  $|p_2| > \omega_t$  the unity-gain frequency  $\omega_t$  can be calculated as

$$\omega_t = a_o |p_1| = \frac{g'_{m2}}{C_M} \quad (8)$$

The phase margin for unity-gain configuration ( $f = 1$ ) is approximately equal to

$$\text{PM} \approx \tan^{-1} \left( \frac{|p_2|}{\omega_t} \right) = \tan^{-1} \left( \frac{g_{m7}}{g'_{m2}} \frac{C_M}{C_L} \right) \quad (9)$$



## 2 Pre-Lab

Using Q2N3904 and Q2N3906 transistors, and assuming  $\beta_{npn} = 140$ ,  $\beta_{pnp} = 180$ ,  $V_{A,npn} = 75 V$ ,  $V_{A,pnp} = 20 V$ , design the two-stage amplifier circuit with the following specifications:

$$\begin{aligned} V_{CC} = V_{EE} = 5 V & \quad C_L = 10 nF \\ R_{E1} = 200 \Omega & \quad a_o \geq 80 dB \end{aligned}$$

1. Show all your calculations and final component values.
2. Find a set of  $C_M$  values which results in  $PM = 30^\circ, 45^\circ$  and  $60^\circ$ .
3. Verify your results using PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
4. Perform AC simulation on the closed-loop circuit in unity-gain configuration for  $PM = 30^\circ, 45^\circ$  and  $60^\circ$ .
5. Apply a 1-V step input and perform transient simulation to obtain the step response for  $PM = 30^\circ, 45^\circ$  and  $60^\circ$ .
6. Submit all simulation plots showing AC and step responses.
7. Be prepared to discuss your design with your TA at the beginning of the lab.

## 3 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.
2. Measure  $I_{supply}$  and all DC quiescent voltages and currents.
3. Observe the frequency and step responses for  $PM = 30^\circ, 45^\circ$  and  $60^\circ$ .
4. Prepare a data sheet showing your simulated and measured values.
5. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.