# FAULT COVERAGE ANALYSIS FOR PHYSICALLY-BASED CMOS BRIDGING FAULTS AT DIFFERENT POWER SUPPLY VOLTAGES

Yuyun Liao
Dept. of Electrical Engineering
Texas A&M University
College Station, TX 77843
Ph: (409)845-9578, Fax: (409)862-2758
email: yliao@cs.tamu.edu

D. M. H. Walker
Dept. of Computer Science
Texas A&M University
College Station, TX 77843
Ph: (409)862-4387, Fax: (409)862-2758
email: walker@cs.tamu.edu

**Abstract**

*Bridging faults in CMOS circuits sometimes degrade the output voltage and time performance without altering the logic function. The traditional voltage testing models based on the normal power supply voltage do not accurately model this behavior. In this paper we develop a model of bridging faults that accounts for both the bridging resistance distribution and gate sensitization and propagation choices. This model shows that fault coverage increases at lower power supply voltages. It suggests that decreasing the power supply voltage is a promising technique to maximize the real fault coverage of voltage tests, thereby minimizing the number of relatively slow Iddq tests required to achieve high quality.*

## 1 Introduction

With the increasing complexity and density of VLSI circuits, shorts between normally unconnected signal lines have become the predominant fault type in CMOS circuits [1]. The shorts can be divided into two subclasses: inter-gate and intra-gate shorts [2], [3]. Inter-gate shorts are usually called bridging faults.

It has been recognized that shorts in CMOS circuits are not modeled adequately by the traditional stuck-at fault model [5], [6]. It has been demonstrated that many shorts are undetectable by functional testing, since some shorts degrade the voltage level and circuit timing performance without altering the logical function. Therefore, much research has been devoted to quiescent current (Iddq) testing as an addition to voltage testing of CMOS circuits to achieve higher test quality [8]-[15]. The primary drawback of Iddq testing with standard ATE is that it is much slower than voltage testing. This usually limits the number of Iddq vectors applied to high-volume chips to 10-20, but often only 1-2 [20], particularly at very low current levels. Newer current sensor designs [10] are much faster, but still much slower than voltage testing. There is also increasing concern that Iddq testing will be less effective in more advanced technologies [11]. In addition, Iddq testing is difficult when the normal Iddq level is high, as is the case in high-performance microprocessors, and many mixed signal devices [23]. For example, a recent implementation of the SPARC architecture has an Iddq of 6 mA [19], and we recently investigated Iddq test of a mixed signal circuit with Iddq currents of 4 mA and greater on each of its multiple supplies. Industrial experience has shown that many chips can be tested at voltages as low as 1.2V, or even lower. This is referred to as "very low voltage" testing [23] or "expanded voltage box" testing [20]. The limit depends on the circuit design techniques and process technology used. The lower the voltage, the better the fault coverage, but even tests at 3V for a 5V part will screen many faults.

The best test strategy should combine both voltage and Iddq tests, but given the speed advantage of voltage testing and existing ATE investment, we should attempt to maximize the real fault coverage of voltage tests, in order to reduce the number of Iddq tests required to target the remaining faults.

In this paper, we investigate the behavior of resistive bridging faults at different power supply voltages from several aspects, such as the maximum detectable resistance, fault coverage, minimum detectable delay increase and fault coverage under different test vector selection strategies. We will show that the detectable range of the bridging resistance and the fault coverage increases significantly as the power supply voltage decreases. Using different power supply voltages for testing has previously been reported in [22]. Very low voltage test has previously been used to detect intra-

gate shorts and hot carrier effects [23], [25].

Early work on bridge fault modeling proposed the "Voting Model" [7]. The shortcoming of this model is that it assumed all gates have the same logical threshold. In order to obtain more accurate simulation results, this approach was further refined to account for varying thresholds [9], [16], [27], [28].

The main drawback of the above models is that they consider the bridging resistance to be negligible. A new parametric model for realistic resistance bridging fault has been proposed [3], [4]. It demonstrated that the classical models such as the "Voting Model" or its refined models developed for non-resistive bridging faults do not adequately represent the behavior of realistic resistive bridging faults. It was shown that even a small realistic resistance can strongly modify the faulty logical behavior. The voltages at bridged nodes depend on the pull-up network, pull-down network, transistor process parameters and bridging resistance ($R_{\rm sh}$). The logic interpretation of the intermediate voltages depends on the configurations of driven gates involved in bridging.

The *input logic threshold* ($V_{\rm th\_in}$) of a gate input is defined as the voltage value at which the input and output of the gate are equal (assuming all other inputs of that gate are held at non-controlling logic values)[26]. A small deviation of the input voltage above or below the $V_{\rm th\_in}$ is sufficient to cause a large swing in the output. The logic interpretation of the intermediate voltages depends on the $V_{\rm th\_in}$ of the driven gates. Each input of each logic gate can have a different input logic threshold. The implication of this behavior is that two driven gates tied to the same bridged node may interpret the same intermediate voltage as two different logic values. This situation has been dubbed "The Byzantine General's problem" [9]. The input logic thresholds for different logic gates can be derived both theoretically and experimentally [26].

Section 2 of this paper describes an analytical model for computing the detectable bridging resistance range at different power supply voltages. Section 3 describes the fault coverage at different power supply voltages. The minimum detectable delay increase at different power supply voltages and test vector sensitivity analysis are investigated in Sections 5 and 6 respectively. Conclusions are given in Section 6.

## 2 Detectable bridging resistance range at different power supply voltages

The whole range of the bridging resistance can be divided into two groups by the maximum detectable resistance $R_{\rm max}$. If the bridging fault resistance falls into the interval [0, $R_{\rm max}$], a functional fault will be exposed at the output of the driven gate, and can be propagated to a primary output. If the bridging fault resistance is greater than $R_{\rm max}$, no functional fault will be exposed at the output of the driven gate, and those faults are classified as *"undetectable"*, since they degrade the circuit performance without altering the logical function. But these faults may cause delay faults.

The detectable bridging resistance range depends

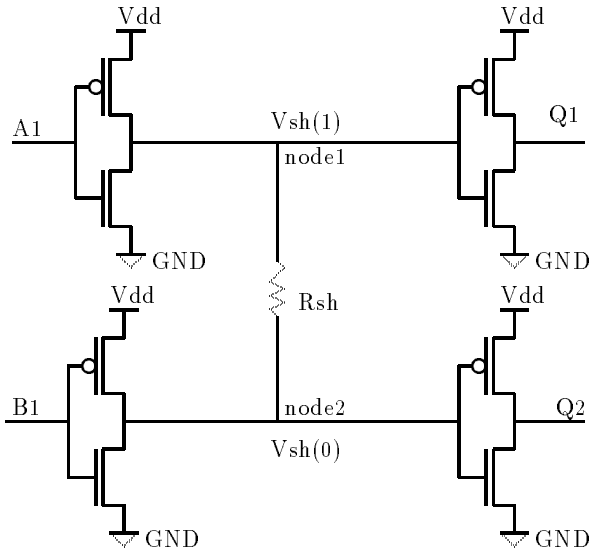


Figure 1: A circuit with bridging fault.

on the bridging configurations and process technology as well as power supply voltage. The bridging configuration shown in Fig. 1 will be used as an example to study the detectable bridging resistance range at different power supply voltages. All circuits used in this paper were constructed using OCTTOOLS [17] standard library cells. All of the HSPICE [18] simulations are based on a $0.8\mu$ N-well CMOS technology.

In order to fully describe the characteristics of a bridging circuit at different power supply voltages, it is necessary to derive the electrical equation to compute $R_{\rm max}$. When the two nodes involved in bridging are set to opposite logic values, the resultant circuit is shown in Fig. 2, assuming A1 = 0 and B1 = 1. In the fault free case ($R_{sh} = \infty$), $V_{sh}(1)$ equals $V_{dd}$ (logic 1). $V_{sh}(1)$ decreases as the value of $R_{sh}$ decreases. If the value of $R_{sh}$ decreases below the value of $R_{\rm max}$, $V_{sh}(1) < V_{\rm th\_in}$ and is interpreted as logic 0. The value of $R_{\rm max}$ can be obtained by writing that $V_{sh}(1)$ is equal to the input logic threshold of the driven gate. The input logic threshold of the inverter (and all other gates) is assumed to be $V_{dd}/2$. Obviously, the two transistors in Fig. 2 operate in their linear regions. The current that flows through the p-transistor, bridging resistance

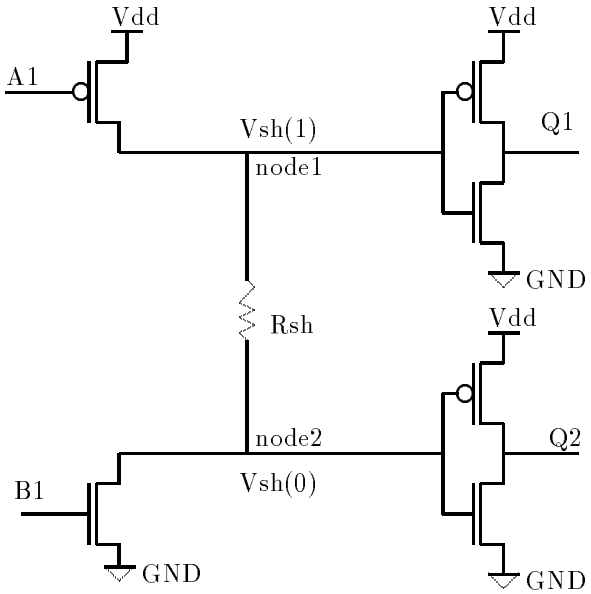


Figure 2: The equivalent circuit of Fig. 1.

and n-transistor is given below:

$$I = \beta_p[(V_{dd} - |V_{tp}|)(V_{dd} - V_{sh}(1)) - \frac{(V_{dd} - V_{sh}(1))^2}{2}] \quad (1)$$

$$I = \frac{V_{sh}(1) - V_{sh}(0)}{R_{sh}} \quad (2)$$

$$I = \beta_n[(V_{dd} - V_{tn})V_{sh}(0) - \frac{(V_{sh}(0))^2}{2}] \quad (3)$$

where:

$$\beta_n = \mu_n C_{ox} W_n/L_n,\ \beta_p = \mu_p C_{ox} W_p/L_p,$$

$V_{tn}$ and $V_{tp}$ are threshold voltages, $\mu_n$ and $\mu_p$ are the respective channel mobilities, $W_n$ and $W_p$ are transistor width, $L_n$ and $L_p$ are transistor length, and $C_{ox}$ is the gate oxide capacitance. For testing based on the evaluation of the $V_{sh}(1)$, $R_{\max}(1)$ can be obtained by substituting $V_{sh}(1)$ by $V_{dd}/2$. $R_{\max}(1)$ is given by:

$$R_{\max}(1) = k_1(\frac{-V_{dd}}{2} + V_{tn} + \sqrt{(V_{dd} - V_{tn})^2 - \frac{2}{k_1\beta_n}}) \quad (4)$$

where:

$$k_1 = 1/[\beta_p((V_{dd} - |V_{tp}|)V_{dd}/2 - {V_{dd}}^2/8)].$$

In the same way, for testing based on the evaluation of the $V_{sh}(0)$, $R_{\max}(0)$ can be obtained by substituting $V_{\rm sh}(0)$ by $V_{dd}/2$. $R_{\max}(0)$ is given by:

$$R_{\max}(0) = k_0(|V_{tp}| - \frac{V_{dd}}{2} + \sqrt{(V_{dd} - |V_{tn}|)^2 - \frac{2}{k_0\beta_p}}) \quad (5)$$

where:

$$k_0 = 1/[\beta_n((V_{dd} - V_{tn})V_{dd}/2 - {V_{dd}}^2/8)].$$

Fig. 3 gives the comparison between the $R_{\max}(1)$ values calculated by equation (4) and the $R_{\max}(1)$ values from HSPICE simulations (using a level2 device model). This figure shows good agreement between the simulations and the proposed equation. From this figure, we know that the detectable bridging resistance range increases as the power supply voltage decreases.

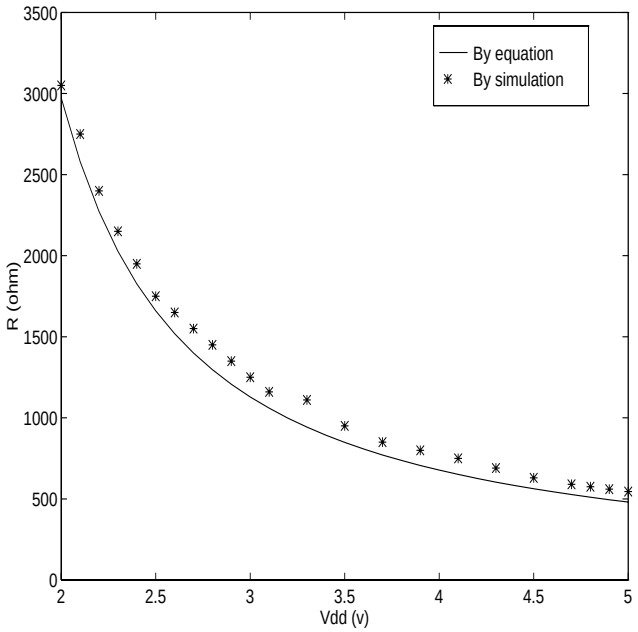


Figure 3: The maximum detectable bridging resistance vs. $V_{dd}$ for Fig. 1.

Note that the analyses above are based the assumption that the input logic threshold $V_{\rm th\_in}$ of the driven gate is $V_{dd}/2$. If the input logic threshold is greater (less) than $V_{dd}/2$, the $R_{\max}(1)$ values will be greater (less) than the values shown in Fig. 3 at different power supply voltages, and the $R_{\max}(0)$ values will be greater (less) than the values calculated by equation (5). In practice, $V_{\rm th\_in}$ is typically in the range of 45 - 55% of $V_{dd}$. This variation can be accounted for similar to the bridging resistance variation in Fig. 4.

## 3 Fault coverage at different power supply voltages

The chief criterion for a test technique is the fault coverage. In this section, we will investigate the fault coverage of the resistive bridge fault model at different power supply voltages. It will be shown that in some cases the fault coverage of a traditional bridge voltage test technique is very low, and the fault coverage increases when the power supply voltage decreases. A CMOS circuit with bridging faults may function correctly at normal power supply voltage, and can be forced to malfunction at a lower power supply voltage. There are two main factors that affect the fault coverage. One factor is the voltages at bridged nodes. The other factor is the input logic threshold of the driven gates.

By means of the maximum detectable bridging resistance $R_{\max}$ computed for each bridging configuration, an accurate fault coverage can be calculated if the bridging resistance distribution is available. Experimental measurements have demonstrated that the metal bridging resistance mainly falls into the range from 0Ω to 1000Ω [1]. A Geometric distribution has been shown [33] to have a good agreement with the data in [1]. One thing we have to mention here is that the bridging resistance distribution depends upon the process technology and the circuit topologies. It is desirable to study fault coverage under different bridging resistance distributions. The distributions shown in Fig. 4 are for several average resistance values, where the middle curve is for the nominal value from [1], and the upper and lower curves are for average resistances ±25% from the nominal value. The actual resistance data will not be as smooth as shown in Fig. 4, particularly high resistance bridges in the tail, but for the purposes of fault coverage estimation, the family of curves is adequate.

The fault coverage of the bridging fault configuration in Fig. 1 at different power supply voltages is given in Fig. 5 along with coverage for different resistance distributions. Note that the coverage reported here is for all bridging faults, not just those causing a functional failure. In this manner, our coverage metric corresponds to Iddq testing, which can detect essentially all bridges between nonredundant nodes. Fig. 5 shows that the coverage increases from 72% at $V_{dd}$ = 5V to 99% at $V_{dd}$ = 2V. The lower the power supply voltage, the high the coverage will be, since a lower power supply voltage will cause a larger fraction of resistive bridges to malfunction. Theoretically, in a complementary CMOS circuit, the power supply voltage can be decreased to slightly higher than the largest threshold voltage of the transistors in the tested circuit. Taking into account the the process variation and other noise sources, the power supply voltage cannot be reduced to the theoretical limit.

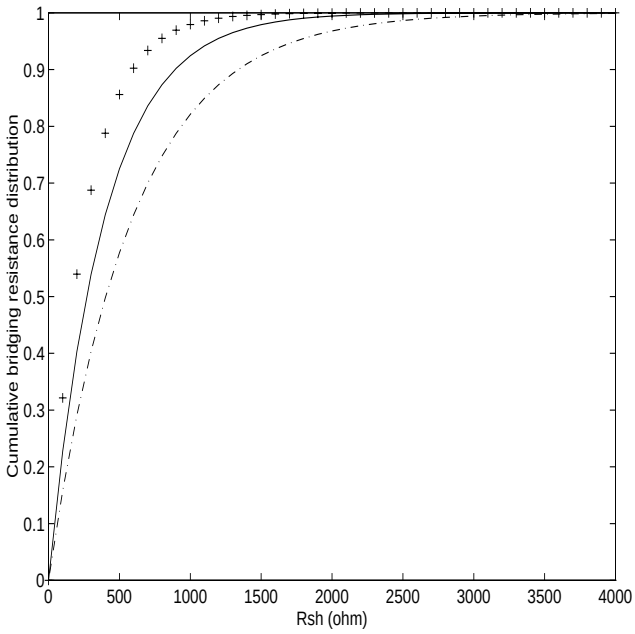


Figure 4: The cumulative bridging resistance distribution. The upper and lower curves are for average resistances ±25% from the nominal value.

## 4 The minimum detectable extra time delay at different power supply voltages

As previously mentioned, if the bridging resistance is greater than $R_{\max}$, it does not alter the logical function. But this fault causes extra time delay (the difference of time delay between the bridging fault and the fault free cases) [24]. Fig. 6 shows the extra time delay caused by the bridging fault in Fig. 1 at different bridging resistances. If the extra time delay exceeds the timing slack on a circuit path, it will cause a delay fault. Obviously, a delay fault can not be detected by traditional stuck-at tests, but can be detected by delay tests [29]-[32].

From the previous section, we know that the delay faults can be forced to malfunction as the power supply voltage decreases. Therefore, the delay faults can be detected indirectly by the low-voltage test technique. The normalized minimum detectable extra time delay $T_{normalized}$ is defined as:

$$T_{normalized} = \frac{T_{extra}}{T_{f\_free}} \qquad (6)$$

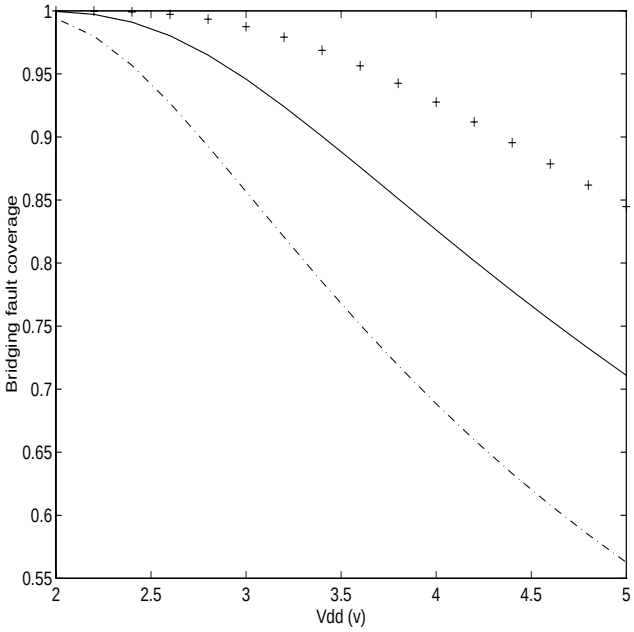


Figure 5: The bridging fault coverage at different $V_{dd}$ for Fig. 1. The upper and lower curves correspond to the lower and upper resistance curves.

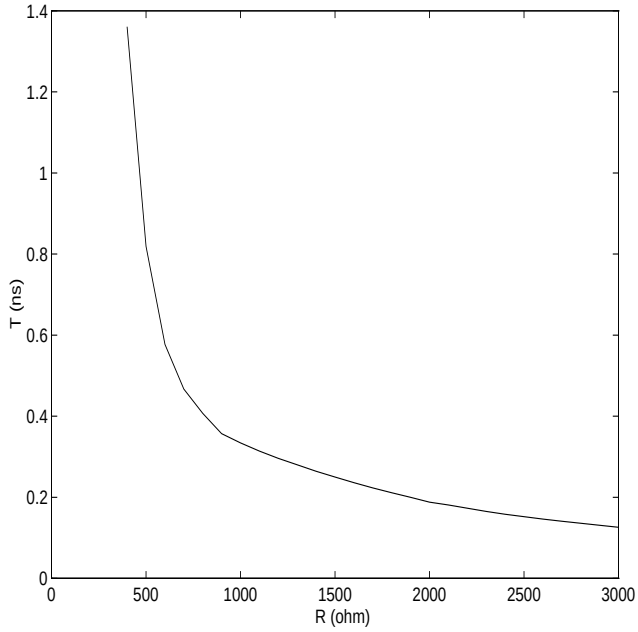


Figure 6: The extra time delay caused by bridging fault vs. $R_{sh}$ for Fig. 1.

where $T_{extra}$ is the extra time delay caused by the bridging faults and $T_{f\_free}$ is the gate delay for the fault free case. By combining Fig. 3 and Fig. 6, the normalized minimum detectable extra time delay caused by bridging faults at different power supply voltages is given in Fig. 7. As can be seen, the minimum detectable extra time delay can be significantly decreased as the power supply voltage decreases. At 5V, $T_{normalized}$ goes to $\infty$, since only functional faults can be detected, and functional faults can be regarded as infinitely slow delay faults. For our example technology, a delay increase of only one gate delay is detectable at 2V. In Fig. 7, all delay increases above the threshold will be detected, even if they do not violate the path slack and cause a delay fault. However, as argued for Iddq testing [21], these "weak" parts are reliability hazards that should be discarded.

Our estimate of the minimum detectable $T_{normalized}$ in Fig. 7 assumes a test speed much slower than typical circuit speeds. If the circuit is tested at reasonable wafer test speeds (e.g. 10-20 MHz), even smaller delay increases will be detectable. One challenge is selecting an appropriate test speed. This can be obtained from a Schmoo plot, or calculated [23], [25]. In practice in industry, a test speed is selected to be low enough to guarantee that no overkill will occur due to tester calibration problems or circuit parametric variations. It is possible to predict the normal circuit speed for a given voltage wafer-by-wafer, allowing dynamic adjustment of the test speed, and a further increase in test coverage [34].

The trend shown in Fig. 7 applies regardless of gate load capacitance. The measurement itself is done at slow speed, and so is relatively independent of interconnect delays. When the interconnect delay is large compared to the gate delay, the trend in Fig. 7 will still apply since higher bridge resistances will result in smaller delay increases, and total stage delay can be increased to infinity for a given bridge resistance by lowering $V_{dd}$ sufficiently.

## 5 Test vector sensitivity analysis at different power supply voltages

If the gate pull-up (pull-down) network has more than one sensitizable path from $V_{dd}$ ($GND$) to the bridged nodes, the test vector is not unique. Consider the circuit shown in Fig. 8. In order to detect a bridging fault, the nodes involved in bridging must be set to opposite logic values. Let us assume that we try to set node 1 to $V_{dd}$, and node 2 to $GND$. To try to set node 1 to $V_{dd}$, $< A1, B1 >$ must be set to $< 0, 0 >$ or $< 0, 1 >$ (vector $< 1, 0 >$ is equivalent to $< 0, 1 >$ and is neglected in this paper). Similarly, to try to set node 2 to $GND$, $< A2, B2 >$ must be set to $< 1, 1 >$ or $< 0, 1 >$ (vector $< 1, 0 >$ is equivalent to $< 0, 1 >$ and is also neglected in this paper). Hence, the pos-

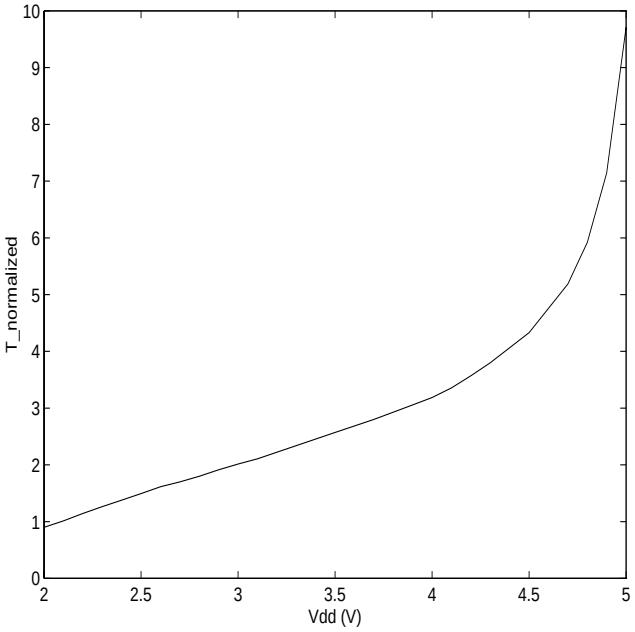


Figure 7: The normalized minimum detectable extra time delay vs. $V_{dd}$ for Fig. 1.

Table 1: The maximum detectable bridging resistances for different test vectors

| test vector A1 B1 A2 B2 | $R_{\max}$ via Q1 | $R_{\max}$ via Q2 |
|---|---|---|
| 0010 | X | 612Ω |
| 0011 | 62Ω | X |
| 1010 | 126Ω | X |
| 1011 | 715Ω | X |

sible values of test vector $< A1, B1, A2, B2 >$ for the bridging fault in Fig. 8 are $< 0, 0, 1, 1 >$, $< 0, 0, 0, 1 >$, $< 0, 1, 1, 1 >$ and $< 0, 1, 0, 1 >$.

The maximum detectable bridging resistance by different test vectors via outputs Q1 and Q2 are given in Table 1, where X indicates that no functional fault is exposed for the bridging resistance range from 0Ω to $\infty\Omega$.

As can be seen, test vector $< 1, 0, 1, 1 >$ and $< 0, 0, 1, 0 >$ are the best candidates for testing via primary output Q1 and Q2 respectively in terms of the maximum detectable bridging resistance.

The bridging fault coverage for the bridging fault configuration in Fig. 8 under different test vectors is given in Table 2. As can be seen, for testing via primary output Q1 in Fig. 8, the bridging fault coverage for test vector $< 0, 0, 1, 0 >$ (a possible choice for traditional test vector selection strategies) is 0.

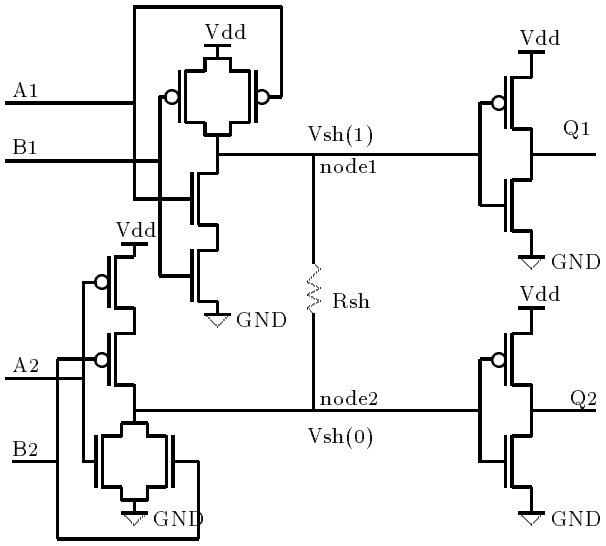


Figure 8: Another example circuit with bridging fault.

Table 2: The bridging fault coverage for the bridging fault configuration in Fig. 8 under different test vectors

| test vector A1 B1 A2 B2 | $C$ via Q1 | $C$ via Q2 |
|---|---|---|
| 0010 | 0 | 81.4% |
| 0011 | 14.8% | 0 |
| 1010 | 27.8% | 0 |
| 1011 | 84.3% | 0 |

There are three test vector selection strategies. The first one is called *Random Strategy* which selects the first test vector found. The second strategy called *Refined Strategy*, which is based on the "Parametric Model", was proposed for realistic resistive bridging faults [3]. The "Parametric Model" can figure out which driven gate will give better fault coverage, but it also uses the first sensitizing test vector found among several candidates. If test vector $< 0, 0, 1, 1 >$ is selected, for example, the "Parametric Model" can figure out that testing via primary output Q1 will give better fault coverage. We assume that each of the possible test vectors has equal opportunity to be selected by the random and refined test vector selection strategies. The last strategy is *the Optimal Test Vector Selection Strategy* [33], which can select the optimal test vector among several candidates in terms of fault coverage. So, for the fault in Fig. 8 the optimal strategy will first try to sensitize the fault with $< 1, 0, 1, 1 >$ and propagate to output Q1. The first two test vector selection strategies suffer from optimism. The fault coverage depends on the selected test vector [33].

The maximum detectable bridging resistance and

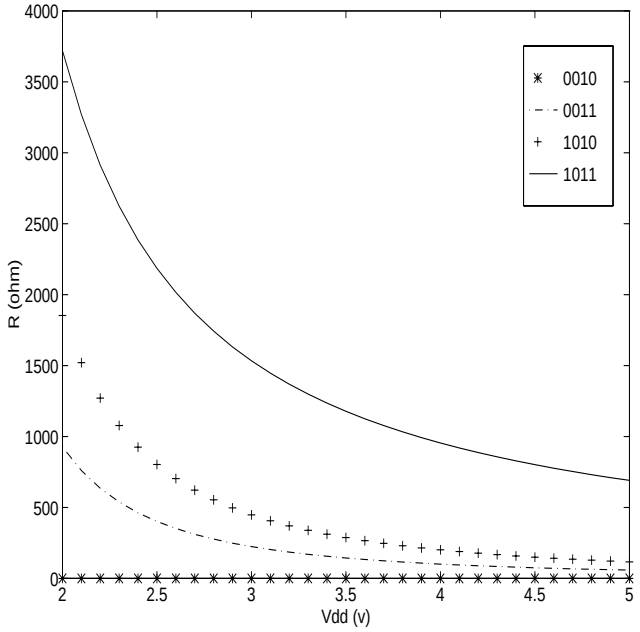


Figure 9: The maximum defect resistance for different test vectors at different $V_{dd}$ for Fig. 8.

fault coverage for different test vectors at different power supply voltages via output Q1 are given in Fig. 9 and Fig. 10 respectively, where the curves on the x-axis indicate that no functional fault will be exposed at primary output Q1 for test vector $< 0, 0, 1, 0 >$. The fault coverage for the different test vector selection strategies at different power supply voltages is given in Fig. 11.

As can be seen, the maximum detectable resistance and fault coverage at different power supply voltages depends on the selected test vector, and the random and refined test vector selection strategies suffer from optimism. But the difference in fault coverage between the optimal and refined test vector selection strategies become small as the power supply voltage decreases. The random strategy is used in industry where the existing functional test set is applied at lower voltage, obtaining a corresponding increase in fault coverage.

Note that our fault coverage estimate is for one vector, and assumes that all sensitizing vectors can be chosen and that a propagation path always exists. For complete test sets on full circuits, it may not be possible to use the best vector, but at the same time, the fault may be detected several times, increasing the real coverage of the random and refined approaches. We are implementing our fault models in a fault simulator to more accurately compute fault coverage.

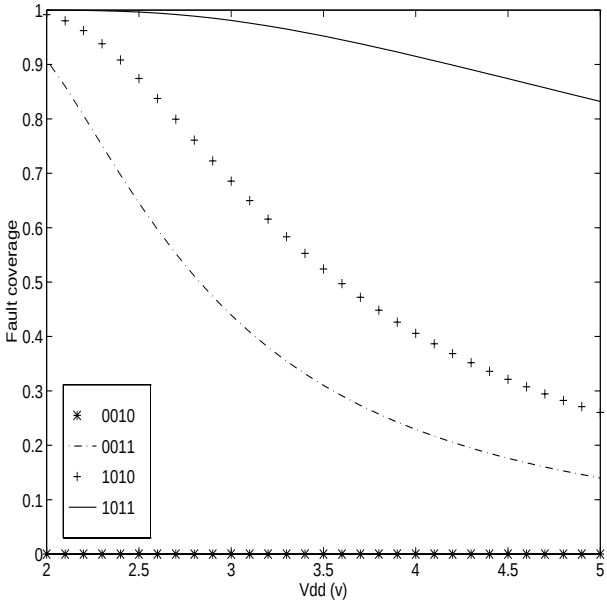


Figure 10: The bridging fault coverage for different test vectors at different $V_{dd}$ for Fig. 8.

## 6 Conclusions and future work

This work has shown that bridging fault coverage and the minimum detectable time delay increase depend strongly on the power supply voltage and the testing vector selection strategies.

Since the bridging faults in CMOS circuits sometimes degrade the output voltage and time performance without altering the logic function, the traditional models based on the normal power supply voltage suffer from lower fault coverage, and result in a higher than expected reject rate. If the optimal test vector selection strategy is used, either the fault coverage can be significantly increased, or a higher power supply voltage can be used to detect bridging faults.

We believe that our approach to low voltage testing obtains many of the benefits of Iddq test, but at higher test speeds. This should reduce the number of Iddq tests necessary to achieve a fault coverage goal. The only requirement is to lower the power supply voltage and the speed of test. But low voltage test speeds will still be much faster than Iddq test speeds, since circuit delay no more than doubles when shifting from $V_{dd} =$ 5V to $V_{dd} = 2$V in complementary CMOS circuits [23]. This is confirmed by Schmoo plots of many industrial circuits.

Our analysis and industrial experience show that the lower $V_{dd}$, the higher the fault coverage. This implies that to make chips more low voltage testable, they should be designed using complementary CMOS, domi-

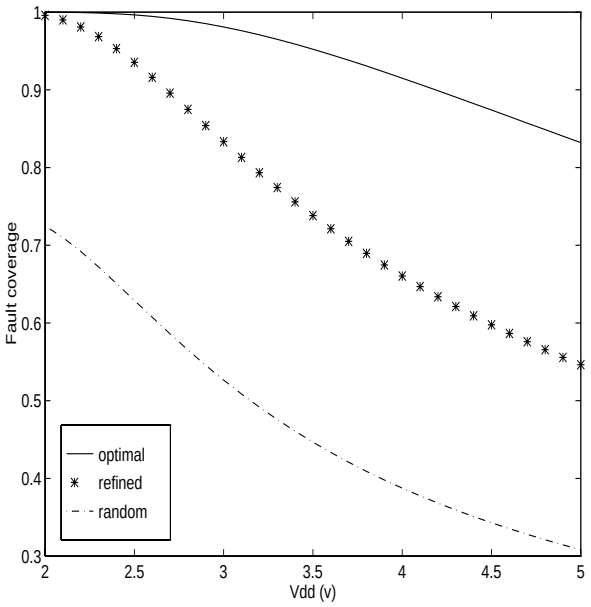


Figure 11: The bridging fault coverage for different test vector selection strategies at different $V_{dd}$.

no CMOS, etc., and should avoid structures such as pass transistors, ratioed logic, etc., that involve transistor threshold drops. Many circuits already meet these requirements, although meeting them may incur a speed penalty. Since transistor threshold voltages are being scaled with supply voltage, low voltage testing will continue to work in the future.

We are currently investigating the floating gate fault behavior at different power supply voltages. We plan to develop new realistic fault models for floating gates and gate oxide pinholes to target the faults missed by traditional test sets.

## Acknowledgments

This research was funded by the Texas Advanced Technology Program under grant 999903-100. The authors would like to thank the reviewers for their valuable comments.

## References

[1] R. Rodriguez-Montanes, E. M. J. G. Bruls and J. Figueras,"Bridging defects resistance measurements in a CMOS process", *Proc. Int. Test Conf.*, pp. 892-899, 1992.

[2] M. Renovell, P. Huc and Y. Bertrand, "CMOS bridging fault modeling", *IEEE VLSI Test Symp.*, pp. 392-397, 1994.

[3] M. Renovell, P. Huc and Y. Bertrand, "The concept of resistance interval: a new parametric model for realistic resistive bridging fault", *IEEE VLSI Test Symp.*, pp. 184-189, 1995.

[4] M. Renovell, P. Huc and Y. Bertrand, "Bridging fault coverage improvement by power supply control", *IEEE VLSI Test Symp.*, pp. 338-343, 1996.

[5] T. M. Storey and W. Maly, "CMOS bridging fault detection", *Proc. Int. Test Conf.*, pp. 842-851, 1990.

[6] T. M. Storey, W. Maly, J. Andrews and M. Miske "Stuck fault and current testing comparison using CMOS chip test", *Proc. Int. Test Conf.*, pp. 311-318, 1991.

[7] J. M. Acken, "Deriving accurate fault models", *Tech. Report CSL-TR-88-365, Comp. Syst. Lab., Stanford*, 1988.

[8] R. Rajsuman, "IDDQ Testing for CMOS VLSI", *Artech House*, 1995.

[9] J. M. Acken and S. D. Millman, "Fault model evolution for diagnosis: Accuracy vs. precision", *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 13.4.1-13.4.4, 1992.

[10] K. M. Wallquist, A. W. Righter and C. F. Hawkins, "A general purpose Iddq measurement circuit", *Proc. Int. Test Conf.*, pp. 642-651, 1993.

[11] W. Needham, "The future of Iddq testing", *Digest of Papers IEEE Int. Workshop on IDDQ Testing*, pp. 2, 1995.

[12] J. M. Soden, and C. F. Hawkins, "Electrical properties and detection methods for CMOS IC defects", *European Test Conference*, pp. 159-167, 1989.

[13] S. D. Millman, and J. M. Acken, "Diagnosing CMOS bridging faults with stuck-at, Iddq, and voting model fault dictionaries", *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 17.2.1-17.2.4, 1994.

[14] M. Keating and D. Meyer, "A new approach to dynamic IDD testing", *Proc. Int. Test Conf.*, pp. 316-321, 1987.

[15] P. C. Maxwell, "The use of Iddq testing in low stuck-at coverage situations", *IEEE VLSI Test Symp.*, pp. 84-88, 1995.

[16] J. M. Acken and S. D. Millman, "Accurate modeling and simulation of bridging faults", *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 17.4.1-13.4.4, 1991.

[17] *OCTTOOLS5.1 User's Manual*, University of California, Berkeley, Oct. 1992.

[18] *HSPICE Manual*, Campbell, Meta-Software Inc., 1990.

[19] L. A. Lev, *et al*, " A 64-b microprocessor with multimedia support", *IEEE J. Solid-State Circuits*, vol. 30, no. 11, pp. 1227-1238, Nov. 1995.

[20] Private communication, U. S. semiconductor manufacturers.

[21] C. Hawkins, J. Soden, " Viewpoint: dealing with yield losses in Iddq testing", *IEEE Spectrum*, vol. 33, no. 1, pp. 68-69, Jan. 1996.

[22] M. W. Levi, "CMOS is most testable", *Proc. Int. Test Conf.*, pp. 217-220, 1981.

[23] H. Hao, E. J. McCluskey, "Very low voltage testing for weak CMOS logic ICs", *Proc. Int. Test Conf.*, pp. 275-284, 1993.

[24] H. Hao, E. J. McCluskey, ""Resistive shorts" within CMOS gates", *Proc. Int. Test Conf.*, pp. 292-301, 1991.

[25] J. T.-Y. Chang, E. J. McCluskey, "Quantitative analysis of very-low-voltage testing", *Proc. IEEE VLSI Test Symp.*, pp. 332-337, 1996.

[26] J. Rearick and J. H. Patel, "Fast and accurate CMOS bridging fault simulation", *Proc. Int. Test Conf.*, pp. 54-62, 1993.

[27] S. D. Millman and J. P. Garvey, "An accurate bridging fault test pattern generator", *Proc. Int. Test Conf.*, pp. 411-418, 1991.

[28] P. C. Maxwell and R. C. Aitken, "Biased voting: a method for simulating CMOS bridging faults in the presence of variable gate logic thresholds", *Proc. Int. Test Conf.*, pp. 63-72, 1993.

[29] G. L. Smith, "Model for delay faults based upon paths", *Proc. Int. Test Conf.*, pp. 342-349, 1985.

[30] J. L. Carter, V. S. Iyengar and B. K. Rosen, "Efficient test coverage determination for delay faults", *Proc. Int. Test Conf.*, pp. 418-427, 1987.

[31] V. S. Iyengar, B. K. Rosen and I. Spillinger "Delay test generation 1 - concepts and coverage metrics", *Proc. Int. Test Conf.*, pp. 857-866, 1988.

[32] W. W. Mao and M. D. Clietti, "A simplified six-waveform type method for delay fault testing", *Proc. 26th Design Autom. Conf.*, pp. 730-733, 1989.

[33] Y. Y. Liao and D. M. H. Walker, "Optimal Voltage Testing for Physically-Based Faults", *IEEE VLSI Test Symp.*, pp. 344-353, 1996.

[34] V. Ramakrishnan and D. M. H. Walker, "IC performance prediction system", *Proc. Int. Test Conf.*, pp. 336-344, 1995.