Estimation of Reject Ratio in Testing of Combinatorial Circuits

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Abstract

Estimating the reject ratio for integrated circuits is an important problem to a test engineer. Using information about the decrease in reject ratio with increasing test length, the test engineer can estimate the test length necessary to achieve a desired product quality goal. In this paper, we suggest a method for estimation of reject ratio for random testing of combinatorial circuits that takes into account differing individual fault probabilities. We also suggest some ways of estimating the fault probabilities. We then demonstrate our method on an example and compare our results to previous work.

1: Notation and Terminology

Total number of stuck-at fault	N
Probability of a random vector detecting stuck-at fault i	$D(i)$
Yield = Probability that no fault occurs on the chip	Y
Test Length	TL
Probability that d defects occur on the chip	$Pr(d)$
Probability of defect size (diameter) being between s and $s+ds$	$h(s)ds$
Critical area for a defect size s for defect type k	$Cr_k(s)$
Probability that d defects cause no stuck-at fault	$NF(d)$
Probability that d defects cause f stuck-at faults	$DF(f, d)$
Given that a single defect causes one stuck-at fault, the probability that the fault is i	$F(i)$
Probability that a chip with j stuck-at faults will escape detection after execution of t tests	$CE(j, t)$
The fraction of the bad chips tested as good after execution of t tests	$FR_{bg}(t)$

2: Introduction

The quality of a test is determined by the *reject ratio* - the fraction of chips that are tested as fault free, but are in fact faulty. Reject ratio is normally estimated from the *fault coverage.* In previous work [29, 33, 21, 1] reject ratios have been estimated from the circuit schematic representation, without any consideration of the actual circuit layout or the manufacturing process. Some consideration to the circuit layout in estimating reject ratio was given in [23]. Different implementations of the same design, or fabrication of the same design on different manufacturing lines, results in different probabilities associated with the *faults*[1] that occur in a chip. Intuitively, it would seem that of two test sequences that have the same coverage, one that covers more of the most probable faults has a better reject ratio. As quality levels of a few parts per million come to be demanded of test engineers, it is our contention that much more information about the circuit, specifically, differing individual fault probabilities, will have to be used in estimating the reject ratios. We quantify this claim by developing a model for estimation of reject ratios for combinatorial circuits, taking into account varying fault probabilities. In doing so we extend work done in [1]. A metric similar to the one we propose in this paper, has been proposed as an improved testability measure for circuits [6].

We begin this paper by identifying the statistics governing the fault and defect density distributions. We then suggest ways by which the individual fault probabilities ($F(i)$) and detectabilities ($D(i)$) can be efficiently evaluated. We develop a model for the reject ratio using the distributions and compare the estimated reject ratio on an example circuit with those predicted by other models. Finally we conclude with ideas for future work.

3: Reject Ratio for Random Testing

The *reject ratio* for a given design is defined as the fraction

1. We use the following convention: Any unwanted particle or liquid droplet that falls on the wafer during manufacturing is called a *contamination.* If the contamination causes any deformation in the form of extra or missing material in some IC layer, a spot *defect* is said to have occurred. Defects are modeled as circles of extra or missing material. *Faults* are functional circuit misbehaviors.

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of chips that pass all tests, but are actually faulty. Let Y represent the actual yield - the fraction of chips that have no faults in them. The yield is a function of the circuit and layout design and the nature and statistics of yield detractors in the manufacturing process. Let $Fr_{bg}(TL)$ be the fraction of total chips that are faulty but escape detection after a test sequence of length TL. The reject ratio is given by

$$R = \frac{Fr_{bg}(TL)}{Y + Fr_{bg}(TL)} \quad (1)$$

We thus need to compute Y and $Fr_{bg}(TL)$ to estimate the reject ratio.

3.1: Fault and Defect Distribution

The primary cause of functional faults in a chip are random local deformations in the form of *defects*. Defects are typically modeled as circles of extra or missing materials in one or more layers of the IC [16].

Whether a defect occurring on a chip causes a fault depends on the defect's size and its position on the chip. Since we model defects as circles, they are completely characterized by two distributions, one governing their spatial distribution and the other governing their size distribution. Any of the reported defect size distributions [25, 9, 26] can be used in our model.

Following Wallmark [31], we assume $Pr(d)$, the probability that d defects occur on the chip to be given by

$$Pr(d) = \frac{\lambda^d \cdot e^{-\lambda}}{d!} \quad (2)$$

λ in the above equation is the average number of defects that occur on a chip (the product of the chip area and the average defect density). Even though we use equation (2) to develop our model, any other expression for $Pr(d)$ can be incorporated in our model. Different types of defects occur on the chip with different frequencies (λ). We will assume that each of these defect types occur independently and follow the distribution in equation (2), but with mean λ_k for defect type k. So the probability that d defects of defect type k, will occur on the chip is given by

$$Pr_k(d) = \frac{\lambda_k^d \cdot e^{-\lambda_k}}{d!} \quad (3)$$

The susceptibility of a design to a defect of a particular defect type and size is characterized by the *critical area* [17, 8, 18, 9]. The critical area for a defect type k and defect size s, $Cr_k(s)$ is defined as that area of the chip where if a defect of type k and diameter s has its center, a fault results. Efficient codes for evaluating the critical area have been reported in [8, 12, 5, 18]. The probability that one defect of type k will not cause any fault is given by

$$NF_k(1) = 1 - \frac{1}{A_c}\int_0^{\infty} h_k(s)\, Cr_k(s)\, ds \quad (4)$$

where $h_k(s)$ is the size distribution for defect type k and A_c is the chip area in the above equation.

It can be shown that the yield of a design [16] can be represented as

$$Y = \sum_{d=0}^{\infty} (Pr(d) \cdot NF(d)) = e^{-\lambda(1-NF)} \quad (5)$$

In equation (5), NF is the probability that a single defect causes no fault. If $NF_k(1)$ is the probability that a single defect of type k causes no fault, assuming that there are a total of M distinct defect types, which occur independently, NF can be represented as $NF = \frac{1}{\lambda} \cdot \sum_{k=1}^{M} \lambda_k \cdot NF_k(1)$, where λ is given by $\sum_{k=1}^{M} \lambda_k$.

The mapping from defects to faults is very complicated. General attempts to evaluate this mapping accurately employ Monte Carlo methods [30]. These are too time consuming to be used to estimate reject ratios efficiently. Faster and simpler methods have been proposed at the cost of generality in [17] and efficient codes for these have more recently been reported in [19]. We will use the model proposed by Seth *et al* [21] to map defects to stuck-at faults. According to this model, the probability of f faults being caused by d defects is:

$$DF(f, d) = \frac{(cd)^f}{f!} \cdot e^{-cd} \quad (6)$$

Parameter c can be evaluated from layout and process information by recognizing that

$$DF(0, 1) = e^{-c} = NF(1) = NF \quad (7)$$

It will be noted that an expression for the yield similar to equation (5), can also be derived from equation (6), by recognizing that yield is also given by

$$\sum_{d=0}^{\infty} Pr(d) \cdot DF(0, d)$$

3.2: Fault Probability Distribution

The faults that can occur on a chip are not equally likely. Global nets are more likely to be involved in a fault than local nets. One can define critical area for individual faults. Given a specified fault, that chip area where if a defect center occurs, the specified fault results, is the critical area for the given fault [5]. One can thus calculate the probability of individual faults. A problem to be overcome here is one of fault mapping. The simulators that give fault probabilities have a different notion of a fault than that used by test engineers. For example, the VLASIC catastrophic yield simulator [30], considers a fault to be a unique topological change to the circuit graph. These faults have to be mapped to the traditional stuck-at fault models in order to use existing fault simulators. There have been attempts at doing this using simulation and heuristics [7, 15, 28].

3.3: Fault Detectability

In order to be able to estimate the test quality, one needs to know the coverage (or expected value of coverage in the case of random testing) as a function of test length. Attempts at expressing this relationship between test length and fault coverage, range from use of semi-analytic functions [10, 33] to estimates based on simulation [2].

In our model, similar to previous researchers, we characterize each fault i with a detection probability $D(i)$. The detection probability is the fraction of total test vectors which detect fault i. One could use any of the methods like PREDICT [22], SCOAP [11], STAFAN [13] and COP [3] to evaluate the detectability of a fault.

3.4: Estimation of Reject Ratio

In this section we attempt to estimate the reject ratio as a function of test length. We do this by first evaluating the probability that a single fault occurring on the chip will escape detection after application of t random test vectors - $CE(1, t)$. Assuming that faults occur independently of each other, the probability that a chip with f faults escapes detection after t test vectors, $CE(f, t)$, under fairly general assumptions, can be shown to be given by

$$CE(f, t) = (CE(1, t))^f \tag{8}$$

The fraction of total chips that have at least one fault on them, but escape detection after t tests, $Fr_{bg}(t)$, is given by

$$Fr_{bg}(t) = \sum_{d=0}^{\infty} \left[Pr(d) \cdot \sum_{f=1}^{N} DF(f, d) \cdot CE(f, t) \right] \tag{9}$$

Let $F(i)$ be the probability that fault i occurs, given that a single fault occurs on the chip. Let $D(i)$ be the detection probability for fault i. The probability that fault i will escape detection after t random test vectors, $E(i, t)$, is given by

$$E(i, t) = (1 - D(i))^t \tag{10}$$

Thus if a single fault occurs on the chip, the probability that t random test vectors will not detect it is given by

$$CE(1, t) = \sum_{i=1}^{N} (F(i) \cdot E(i, t)) \tag{11}$$

From equations (9), (8) and (6) we get

$$Fr_{bg}(t) = \sum_{d=0}^{\infty} Pr(d) \cdot e^{-cd} \cdot \sum_{f=1}^{N} \frac{(cd \cdot CE(1, t))^f}{f!} \tag{12}$$

Assuming N is large enough, a realistic assumption for typical circuits, the second summation can be replaced from $f = 1$ to N to $f = 1$ to ∞. The second summation in equation (12) is then the Taylor series of an exponential. Equation (12) can thus be simplified to

$$Fr_{bg}(t) = \sum_{d=0}^{\infty} Pr(d) \cdot e^{-cd} [e^{(cd \cdot CE(1, t))} - 1] \tag{13}$$

From equations (2) and (13), we get

$$Fr_{bg}(t) = \sum_{d=0}^{\infty} \frac{\lambda^d \cdot e^{-\lambda}}{d!} \cdot (e^{-cd(1 - CE(1, t))} - e^{-cd}) \tag{14}$$

Substituting the value of e^{-c} from equation (7), the above equation can be simplified to

$$Fr_{bg}(t) = e^{-\lambda} \cdot (e^{\lambda \cdot (NF)^{(1 - CE(1, t))}} - e^{\lambda \cdot NF}) \tag{15}$$

This expression for the fraction of chips that have at least one fault in them but escape detection, reduces to the expression obtained by several previous researchers [21, 1] if one assumes that all faults are equally likely.

Let us assume that the test length is TL. The chips that are fabricated fall into one of the following categories:

1. Chips that do not have any defect on them. The fraction of total chips that fall into this category, from equation (2), is given by $Pr(0) = e^{-\lambda}$.
2. Chips that have some defects on them, but none of

these defects cause any fault. The fraction of the chips that fall into this is $e^{-\lambda} \cdot (e^{\lambda \cdot NF} - 1)$.

3. Chips that have some defects on them, with at least one fault. The fraction of chips that have a fault but escape detection is given by equation (15).

For a given test length *TL*, substituting in equation (1), the values of $Fr_{b_g}(TL)$ from equation (15) and yield from equation (5), we get the expression for reject ratio as:

$$R(\lambda, NF, TL) = 1 - \left(\frac{e^{NF}}{e^{(NF)^{(1-CE(1,TL))}}}\right)^{\lambda} \quad (16)$$

The reject ratio can thus be computed purely from circuit schematic and layout information and defect statistics. It should also be noted that the various distributions assumed are not critical to the development of the model.

Since the yield is a more directly observed parameter, we can replace λ in equation (16) by using equation (5) to give

$$R(Y, NF, TL) = 1 - \left(\frac{e^{NF}}{e^{(NF)^{(1-CE(1,TL))}}}\right)^{-\frac{\log Y}{(1-NF)}} \quad (17)$$

4: Example

In order to demonstrate the differences in our model for reject ratio and the traditional models we consider as an example a CMOS 15-to-4 priority encoder circuit. The encoder was implemented in a 1μm double-metal, single-poly, P-well CMOS process. Figure 1 shows the layout of the example circuit. The dimensions of the layout are 723μ by 303μ. This circuit has a total of 15 input nodes, 4 output nodes and 53 internal nodes for a total of 72 nodes. Assuming a s-a-0 and s-a-1 fault at every node and a Vdd to Ground short fault, gives us a total of 145 faults.

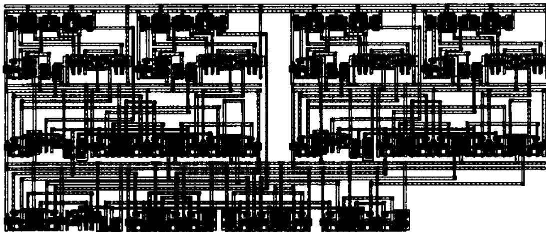

Figure 1 : Layout of the example circuit

For the purposes of this experiment, the detectability *D(i)* of each fault was computed by performing a fault simulation [14] on a sample of randomly generated test vectors. The fault simulator was queried at the end of each fault simulation run for the stuck-at faults detected by that test. The fraction of the total number of times a fault was detected to the total number of test vectors is then a measure of the detectability of that fault. Figure 2 shows the detectability of the faults indexed in increasing order of their detectability. Since the circuit under consideration is a priority encoder, we have faults with a wide range of detectability. A stuck-at-0 fault in the most significant input bit is detected by half the possible test vectors, while a similar fault in the least significant input bit will be detected by just one test vector.

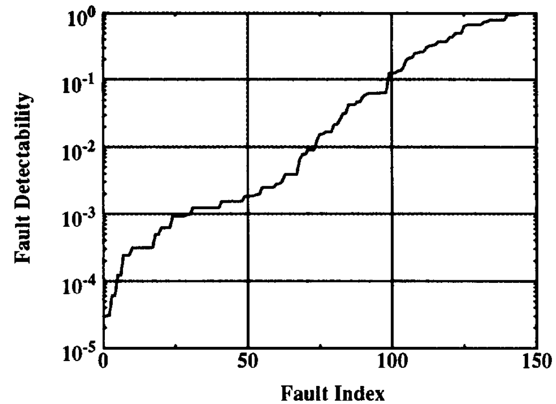

Figure 2 : Detectability of Faults for the Example Circuit

The VLASIC catastrophic yield simulator [30] was used to compute the fault probabilities. For simplicity, only extra metal defects were assumed to affect the circuit. It will be noted that the reject ratio model we have derived in the previous section makes no such assumption. We, thus, have to consider only node shorts. One million extra metal defects were introduced each in the first and second metal layers, using the size distribution in equation (18) [9, 27].

$$h(s) = s_0^2/s^3 \ \forall (s > s_0) \quad (18)$$

s_0 in equation (18) is typically much smaller than the smallest defect that can cause a fault.

The node shorts needed to be mapped to the stuck-at fault model. The reason for requiring such a mapping is again a feature of the tool we used to compute fault detectabilities. Since the fault simulator used a stuck-at fault model, we were required to map the bridging faults reported by VLASIC to the 145 stuck-at faults used in the fault simulator. In performing this mapping we made the following assumptions:

1. A short between two or more nodes, not involving either Vdd or Ground, is equally likely to cause a stuck-at fault at each of the participating nodes. The

mapping from node pair shorts to stuck-at faults has been investigated [28] to find what fraction of faults map to stuck-at faults. Our assumption of a node short being equally likely to cause a stuck-at fault at either of the nodes can thus be verified or altered.

2. A short between two or more nodes, not involving either Vdd or Ground is equally likely to cause a stuck-at-0 and a stuck-at-1 fault on the shorted nodes. Clearly this is not true in all cases. A n-channel FET source-drain short, for example, is equivalent to the gate stuck-at-1. However this type of fault does not occur in the example circuit.

3. Any node besides Vdd or Ground, shorting to Vdd or Ground causes a stuck-at-1 or a stuck-at-0 fault on that node respectively.

4. A short between Vdd and Ground is a special kind of fault, with a detectability of one. This assumption implies that any test will detect a short between Vdd and Ground.

The assumptions can be modified as necessary to provide a more realistic mapping. Note that, if fault simulators with more sophisticated fault models were available, such as bridging faults, one could dispense with the above assumptions.

Based on the assumptions discussed above, fault probabilities for individual stuck-at faults were calculated. The VLASIC simulation, thus, not only gave an estimate of the *NF*, but also helped estimate the individual fault probabilities $F(i)$. Assuming that extra metal defects have the same size and spatial distributions in both metal layers, the value of *NF* was determined to be 0.814. Figure 3 shows the individual fault probabilities. (It is important to note that in both Figures 2 and 3, the fault detectabilities and probabilities have been sorted in the increasing order, so the fault indices for the two graphs are not correlated).

Figure 3 shows the reject ratio as a function of test length for different values of predicted yields using the values of $D(i)$ and $F(i)$ calculated above. (The values of yields chosen for the graph correspond to defect densities of 2 to 20 defects per cm^2) As expected, a larger defect density, which corresponds to a lower yield, causes a higher reject ratio for a given test length.

Figure 5 shows the percentage difference between the reject ratios estimated by different models and our model as a function of test length, for the example with a 99% yield.

Model 1 is our mode - equation (16). Model 2 is the same model as model 1, except that we assume that all the faults are equally likely. This model is equivalent to the one developed in [1]. Model 3 is the one developed by Wad-

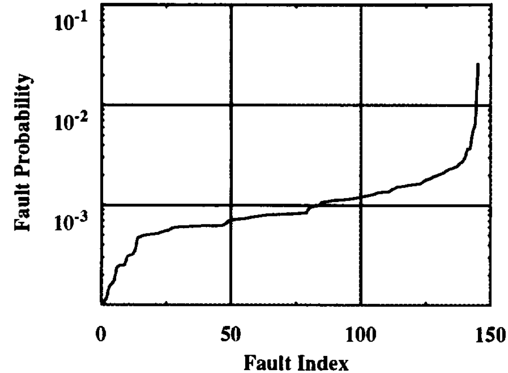

Figure 3 : Probability of Fault Occuring for the Example Circuit

sack [29]. This model assumes that the reject ratio is given by

$$R = (1 - cov)(1 - Y) \qquad (19)$$

Model 4 is the one described by Williams and Brown [32]. This model assumes that the reject ratio is given by

$$R = 1 - Y^{(1 - cov)} \qquad (20)$$

cov in equations (19) and (20) is the fault coverage.

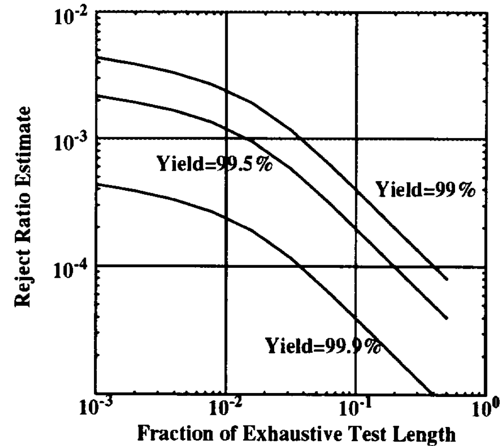

Figure 4 : Reject Ratio Estimates for Different Values of Yield for the Example Circuit

It can be seen that the reject ratio predicted by our model is consistently smaller than that predicted by the other models. This feature of the model can directly be traced to dispensing with the assumption of equal fault probability. It will also be noted, that as the test length and consequently the fault coverage increases the discrepancy between the reject ratio predicted by our model and the traditional mod-

els also increases. It is in this region - one with very high fault coverage - that a test engineer is typically interested in an accurate estimate of the reject ratio. It is important to note that all the parameters for our model are directly observable and thus the reject ratio can be estimated a-priori.

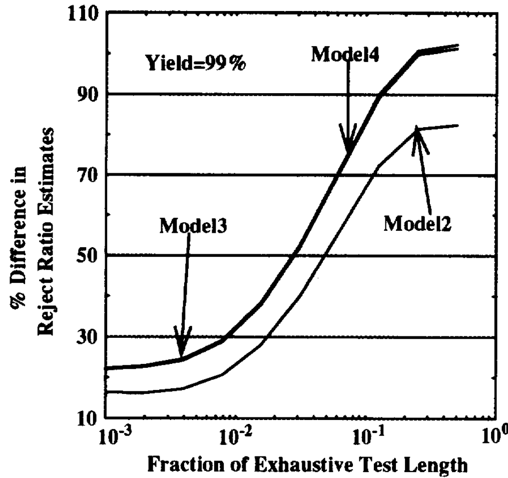

Figure 5 : Comparing Estimated Reject Ratios of Different Models

Models 1 and 2 predict different values of reject ratio because they estimate *CE(1, TL)* differently. *CE(1, TL)* is the probability that a chip with one fault escapes detection after application of *TL* random test vectors. Traditional reject ratio estimation models, specifically model 2, associate *CE(1, TL)* with *(1 - cov)*. Having weighted each fault with its probability of occurence *F(i)*, we have come up with a more physical description of fault coverage. If the fault probability *F(i)* and fault detectability *D(i)* were completely uncorrelated, the value of *CE(1, TL)* predicted by our model would be the same as predicted by assuming faults to be equally likely. Intuitively, one would expect some correlation between *F(i)* and *D(i)*. Faults more likely to occur on the chip are also more likely to be more detectable (e.g. faults involving global nets).

Figure 6 shows the estimated fault escape *CE(1, TL)*, with and without the assumption of equal fault probability. As will be observed from the figure, the difference between the predicted values of *CE(1, TL)* increases as the test length increases.

5: Conclusions and Future Work

In this paper, we have shown that using individual fault probabilities can result in up to a 100% difference in the estimated reject ratio. By considering individual fault probabilities, our model achieves a closer approximation to the physical reality than conventional models. Since

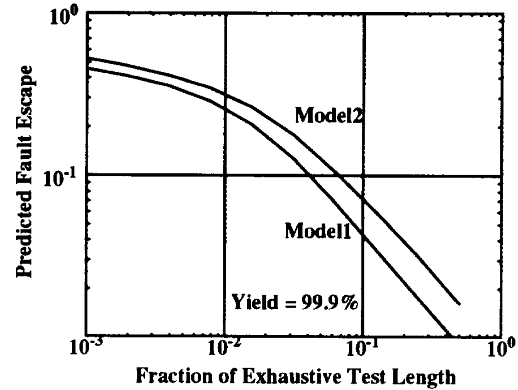

Figure 6 : Comparing Estimated Fault Escape - *CE(1,TL)* of Different Models

testing constitutes a significant fraction of the total manufacturing cost for a design, a better estimate for reject ratio implies a better estimate of the test length required to achieve desired quality levels.

In this work we have used knowledge of the process flow, defect statistics and mask artwork to obtain fault probabilities. It is often the case that an estimate of reject ratio as a function of test length is required much earlier in the design process, for example in the design of BIST [33]. One possible solution is to extract the λ_k, $Cr_k(s)$ and $h_k(s)$ characteristics for common process flows, design styles, module types and typical defect statistics, so that equation (16) can be applied before layout design has been completed. As more design and process information becomes available, a more accurate reject ratio estimate can be made.

In this paper we have assumed a Poisson distribution for the defect spatial distribution (equation (2)). We could consider a more realistic distribution, such as the negative binomial [24]. We also assumed that the mapping from the number of defects to the number of faults is given by equation (6). VLASIC and other Monte Carlo layout simulators have the capability of directly computing this relationship.

In this work we have assumed a random test sequence applied to combinatorial logic. Two important ways in which this model can be improved are in considering deterministic testing and testing of sequential circuits. Attempts at understanding how deterministic testing and testing for sequential circuits alter the assumptions made in this paper have been reported in [20] and in [4] respectively.

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