Timing Analysis of Combinational Circuits Including Capacitive Coupling and Statistical Process Variation

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Abstract

Capacitive coupling between interconnects can lead to pattern-dependent delay variation. Statistical process fluctuations result in variation in gate and interconnect delays, and interconnect coupling. These effects become increasingly important in deep submicron circuits. In this work we describe a statistical timing analyzer for combinational circuits that takes these effects into account. The tool searches for input vectors that sensitize the longest path and maximizes the delay on these paths due to capacitive coupling. The best and worst-case timing on the paths is then computed using random gate delay variation and spatially-correlated interconnect parasitic variation. We demonstrate timing analysis results on a subset of the ISCAS85 circuits.

1. Introduction

A significant problem in accurate timing analysis and delay test generation is that the effective load capacitance seen by a gate is dependent on the switching activity of nets that are capacitively-coupled to the gate output. If two coupled nets switch in the same direction (helper), they can have lower signal delay. If they switch in the opposite directions (aggressor), they can have longer signal delay. [1,2]. As a result, circuit delay is dependent on the input patterns [3,4,5,6]. Traditional path delay test generation [7,8,9,10,11] does not consider this capacitive crosstalk. In order to ensure that path delays are maximized, timing analysis and test generation should constrain the search space so that aggressive transitions on coupled nets are sensitized. Previous work on capacitive crosstalk has focused on maximizing the local noise so as to induce logic faults, rather than consider path delay faults [12,13,14,15]. The exception is the work described in [16], which does not consider process parameter correlation.

Statistical process variation is another source of delay variation. Process parameters can vary as much as +/–30% with random intra-die variations exceeding +/–10% [17], and results in corresponding path delay variation [18,19]. A delay model that only considers the uncorrelated best/worst-case gate delays would result in circuit delay values that are much larger than the real best/worst case.

Our proposed statistical timing analysis (STA) methodology determines +/-3σ limits on delay variation of the critical paths due to signal coupling and process parameter variation. Ideally process correlation is taken into account when searching for signal couplings, since the correlation will eliminate some couplings and increase the effect of others. However, to minimize algorithm complexity, the input vectors to sensitize the longest paths and the worst-case coupled transitions are computed first. The maximum delay on these paths is then computed over the range of process variation.

This paper is organized as follows: in section 2 we describe the delay model, path sensitization criteria, and a model for effective coupling capacitance. In section 3 we explain the generation of worst-case capacitive couplings on the longest sensitizable paths. In section 4 the proposed STA methodology is formulated. In section 5 we present results for some test circuits. Finally, in section 6 we draw conclusions and discuss future work.

2. Delay Models

Statistical timing analysis requires identification of the potentially longest sensitizable paths in the circuit. Our search procedure [20] uses a min-max gate delay model [21,22,23] with separate bounds for rising and falling transitions. In order to ensure that all potentially longest paths are identified, the delay bounds include the variation caused by the best and worst-case capacitive couplings and ±15% delay variation caused by process variation.

Timing simulation with the min-max delay model produces an uncertainty interval (UI) [24,25] in the gate output transition. If the gate has a minimum delay g(l) and a maximum delay g(u) and the input transition occurs between t1 and t2, then the output transition occurs in the interval [t1 + g(l), t2 + g(u)]. Thus the UI expands as a signal propagates along the path. We assume that local process variation is large enough that we can approximate the transition as occurring uniformly in the UI, and with low correlation to transitions on neighboring gates.

A path is said to be sensitizable if an input pattern can propagate the signal from a primary input to a primary output through the path [22]. In this work we use the

dynamic sensitization criterion [9,10,11], which allows transitions on the side inputs. We only consider two-pattern tests. If a path is sensitizable in the entire range of the UI at the primary output of the path, then the path is said to be *always sensitizable* (AS). If a path is sensitizable only in for a subset of the final UI, then the path is said to be *sometimes sensitizable* (SS) [20]. In other words, the path is sensitizable for a subset of the process parameter values or possible coupling conditions. To make a path AS, side input constraints (SIC) must be set on the side inputs of each gate on the path so that the entire UI of the on-path transition propagates through each logic stage. To make a path SS, a non-controlling value must be set on side inputs in order to propagate a minimal duration glitch (as determined by gate inertial delays).

Figure 1 shows the SIC for falling and rising on-path transitions for a two-input AND gate with a as the on-path input and b as the side input. For the AS condition, b must be held high until after it is certain that a has fallen. For the SS condition, b can fall any time after a might have fallen. The gate inertial delay (δ) is added to the SIC to ensure signal propagation when a transitions to a non-controlling value. The AS criterion guarantees that the transition during the UI is the last one on the path and that glitches cannot propagate. Under the SS criterion, both glitches and multiple transitions can propagate on the path.

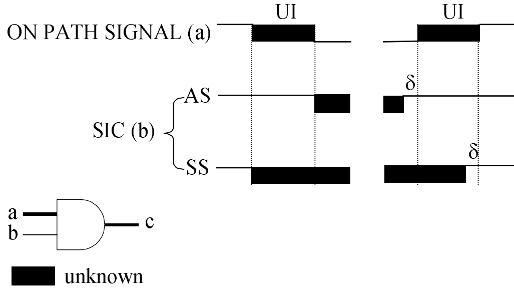

Figure 1. Always (AS) and Sometimes Sensitizable (SS) SIC for 2-input AND gate.

For each gate type, the delay is a function of the transition direction, process parameters, the on-path input transition time t_{in}, the output load resistance R_L, and the output load capacitance C_L. These functions are computed by fitting low-order polynomials to circuit simulation data [26]. The load capacitance is computed as:

$$C_L = C_{ii} + \sum_{j=1, i \neq j}^{k} \alpha_{ij} C_{ij} \quad \text{(Eq. 1)}$$

where C_{ii} is the capacitance to ground of net i on the path, C_{ij} is the coupling capacitance of net j to net i, α_{ij} is the *effective coupling capacitance factor* (ECCF) based on the switching activity on nets i and j, and k is the number of nets coupled to i. If the exact transitions on coupled nets are known, the ECCF can be accurately computed [16]. However due to intra-die process variation, the exact time of signal transitions is not known. A min-max ECCF could be computed but this will lead to unrealistic delay bounds. Instead we use a probabilistic linear model based on the *overlapped UIs* (OUI) of the coupled transitions.

The ECCF for the aggressor coupling shown in Figure 2 is calculated as:

$$ECCF_a = 1 + \frac{OUI_{AB}}{UI_A UI_B} \quad \text{(Eq. 2)}$$

where $UI_A = t_3 - t_1$ is the UI of signal A, $UI_B = t_4 - t_2$ is the UI of signal B, $OUI_{AB} = t_3 - t_2$ is the OUI of A and B, and $1 \le ECCF_a \le 2$. The ECCF for the helper case is:

$$ECCF_h = 1 - \frac{OUI_{AB}}{UI_A UI_B} \quad \text{(Eq. 3)}$$

where $0 \le ECCF_h \le 1$. Intuitively the larger the OUI_{AB} and the smaller the UI_A or UI_B, the larger the ECCF.

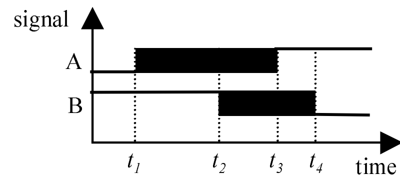

Figure 2. Two Aggressively Coupled Signals with UIs.

Our ECCF model assumes that nets have similar transition times. If the coupled net has a much faster transition time than the on-path net, then an ECCF greater than 2 can result. Our ECCF model also neglects driver and interconnect resistance. However Monte Carlo circuit simulation shows that our ECCF model is fairly accurate over a range of gate and interconnect parameters [27].

Table I shows all signal coupling cases for a rising on-path transition (S_{ir}). If a coupled signal is stable 0 or 1 (S_{j1} and S_{j2}), it is considered a virtual ground (ECCF=1). Cases S_{j3} – S_{j6}, are aggressors and the ECCF is calculated using Eq. 2. Cases S_{j7} – S_{j10} are helpers and the ECCF is calculated using Eq. 3. If a coupling transition is one of S_{j11} – S_{j13}, the coupled net has no constraint. Cases S_{j12} and S_{j13} occur when more than one SIC is required on the same net. Cases S_{j11} – S_{j13} are used by the statistical timing analyzer to search for the worst-case couplings by assigning the sensitizing signals on the unconstrained coupled nets.

3. Path and Coupling Generation

We incrementally generate the longest sensitizable paths with the min-max delay models using the static timing analyzer approach described in [20]. The primary challenge is then to search for an input pattern that causes transitions on coupled nets that maximize the path delay under the AS or SS sensitization criteria. The generated input pattern is a two-pattern transition-mode vector. The algorithm for each path is shown in Figure 3. For each net i on the path, all coupled nets j with a signal of case S_{j11}, S_{j12} or S_{j13} in Table I are considered. These are the

unconstrained nets where transitions can be set to maximize the path delay. Nets whose coupling capacitance is not significant (more than 5% of the total net *i* capacitance) are discarded.

Table I. All Possible Signal Couplings for a Rising On-path Signal and Their ECCF.

Signal		Tran.	ECCF	Description
	S_{ir}	RT	-	On-path Signal
	S_{j1}	S0	1	Constant 0
	S_{j2}	S1	1	Constant 1
	S_{j3}	FT	[1 2]	Early Falling Tran.
	S_{j4}	FT	[1 2]	Falling Tran. inside UI
	S_{j5}	FT	[1 2]	Late Falling Tran.
	S_{j6}	FT	[1 2]	Falling Tran. with Wider UI
	S_{j7}	RT	[0 1]	Early Rising Tran.
	S_{j8}	RT	[0 1]	Rising Tran. inside UI
	S_{j9}	RT	[0 1]	Late Rising Tran.
	S_{j10}	RT	[0 1]	Rising Tran. with Wider UI
	S_{j11}	U	[0 2]	Unassigned
	S_{j12}	U	[0 2]	Don't Care of Partial 0 SIC
	S_{j13}	U	[0 2]	Don't Care of Partial 1 SIC

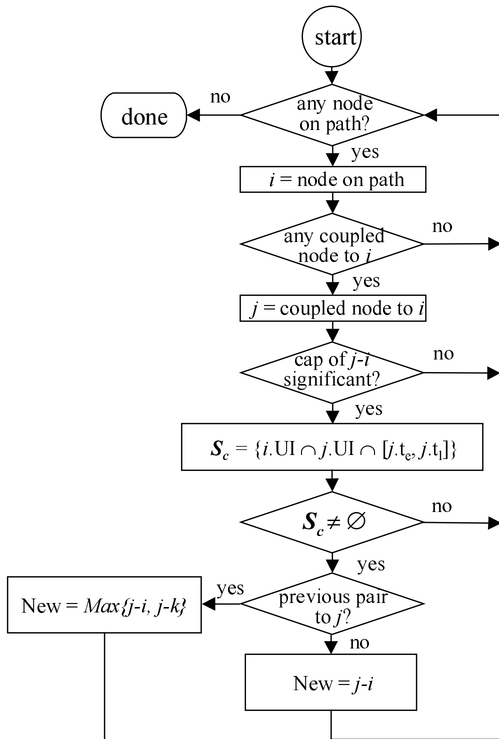

Figure 3. Procedure to Search for the Worst Case Capacitively Coupled Signals.

The required coupling signal (S_c) to maximize delay is then computed as shown in Figure 4. The coupled net must have a transition opposite that of the on-path transition (S_i) to create an aggressor case. In order for the transitions to be coupled, he UI of the coupled nets must overlap with the UI of S_i. In order to maximize the ECCF, the UIs should exactly overlap. This is constrained by the earliest and latest arrival time for a transition on net *j*, which is represented by the interval [t_e(j) t_l(j)]. In cases where a net *j* couples to several nets on the path, only the net with the largest coupling capacitance to *j* is used to compute S_c. This is incorrect if many small aggressors create a larger delay increase than one large aggressor. However in inverting logic stages, additional coupling capacitances from net *j* to the path are as likely to be helpers as aggressors, and so their delay impact will tend to cancel.

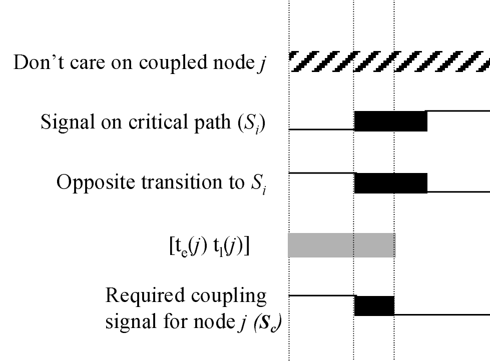

Figure 4. Required Coupling Transition for the Unassigned Coupled Nets.

Given the required coupling transitions, the next step is to try to sensitize each coupling case on the path. We use a greedy approach of considering couplings in decreasing order of their delay increase, using the FAN algorithm [28] for justification. The greedy approach can miss the case where several small couplings result in a larger delay than one large coupling. This is likely only when the coupled signals are correlated, such as a bus crossing over a net.

One concern when assigning transitions to coupled nets is whether this alters the path sensitization. Under the AS criterion, the valid combination of signal transitions on coupled nets cannot alter the path sensitization since the path delay varies only in the UI of the final transition of the primary output. This is not true for the SS criterion, and this can result in the path no longer being sensitizable. The result is that the timing analyzer may report timing on a path that is not sensitizable for the predicted input pattern, although it may be sensitizable for another pattern. An example of this is shown in our experimental results. The impact is that we may overestimate circuit delay.

To limit the algorithm complexity, we do not consider delay variation on side input or coupled signals due to coupling on their paths. This variation could result in a path not being sensitizable, or else having a delay smaller

than predicted. Examples of this are shown in the experimental results. One possible solution is to incorporate additional logic and timing constraints into the path search process, but this is likely to be either greedy (e.g. propagate constraints based on a partial input vector), or require many backtracks to find a global worst case.

4. Statistical Timing Analysis

We have developed a STA methodology to find the delay variation of the generated critical paths due to process variation, including intra-die process variation. In order to avoid a nonlinear optimization problem [26], we approximate the circuit delay as linear in the process parameters. This is fairly accurate for the process parameters of interest. Interconnect segments between gates are defined as elements of the problem whose parameters can vary, and interconnect parameters such as metal width and thickness, and interlayer dielectric (ILD) thickness are defined as element parameters. (We did not consider variation in gate internal delay. We have previously developed a delay test ATPG for delay faults caused by affected by gate delay variation [26], but have excluded it here to simplify the initial phase of this research). The element process parameters are modeled as having an intra-die variation consisting of a distance-based gradient variation and random Gaussian noise.

The computation finds the plane (gradient across the chip) for each process parameter that maximizes or minimizes the path delay, the delay value, and the path element values. The inputs to the procedure are the sensitivity of path delay, S_{ij}, to process parameter i in element j located at $<X_j, Y_j>$, the plane parameters for process parameter i, A_i and B_i, which are bounded by a min-max range, standard deviation of element parameter σ_{ij}, and covariance $Cov(\Delta P_{ij}, \Delta P_{ik})$ or correlation coefficient ρ_{ijk} for elements j and k for parameter i. Covariance and correlation coefficients may be given, or else derived from minimum σ_{ijk}, the minimum element parameter variance (due to intra-element variations), and D_i, the rate at which the standard deviation of the difference between two element parameters rises with distance [29]. The outputs are the +/- 3σ path delays and the gradient coefficients, A_i and B_i that achieve this. The formula of parameter variation can be split into gradient and random factors as follows:

$$\Delta P_{ij} = A_i X_j + B_i Y_j + N(0, \sigma_{ij}^2) \quad \text{(Eq. 4)}$$

where P_{ij} is a value of parameter i in element j, A_i and B_i are the distance-based gradient of parameter i in X and Y direction, respectively, $<X_j, Y_j>$ is the location of element j, and σ_{ij} is the standard deviation of parameter i in element j. Then performance F is defined as:

$$F = F_n + \Delta F = F_n + \sum_{ij} S_{ij} \Delta P_{ij} \quad \text{(Eq. 5)}$$

where F_n is the nominal performance and ΔF is the performance variation. By taking the derivative of ΔF w.r.t. A_i and B_i, we can determine gradients to maximize or minimize F. The gradients to maximize F are A_{Mi} and B_{Mi}. Then maximum F is formulated as:

$$F_M = F_n + \sum_{ij} S_{ij}(A_{Mi} X_j + B_{Mi} Y_j) + \sum_{ij} S_{ij} N(0, \sigma_{ij}^2) \quad \text{(Eq. 6)}$$

The gradient part of F_M is:

$$F_{Mg} = F_n + \sum_{ij} S_{ij}(A_{Mi} X_j + B_{Mi} Y_j) \quad \text{(Eq. 7)}$$

The minimum F, F_m, is computed by substituting A_{mi} and B_{mi}, the X and Y direction gradients for minimum F, into Eqs. 6 and 7. The standard deviation of F is:

$$\sigma_F = \sqrt{\sum_{ij} S_{ij}^2 \sigma_{ij}^2 + 2\sum_{ij} \sum_{k=j+1} S_{ij} S_{ik} Cov(\Delta P_{ij}, \Delta P_{ik})} \quad \text{(Eq. 8)}$$

where $Cov(\Delta P_{ij}, \Delta P_{ik}) = \sigma_{ij}\sigma_{ik}\rho_{ijk}$. The maximum F in the 3σ range is:

$$F_M = F_{Mg} + 3\sigma_F \quad \text{(Eq. 9)}$$

The minimum F in the 3σ range is:

$$F_m = F_{mg} - 3\sigma_F \quad \text{(Eq. 10)}$$

The performance change due to a parameter can be computed by considering only a single parameter *i* in Eqs. 4 to 8. A complete description of the statistical analysis can be found in [27].

5. Implementation and Results

The proposed methodology was implemented with ISCAS85 benchmark circuits. Layouts were generated in a triple-metal 0.25 μm (L_{eff}) CMOS Nwell technology using the Cadence LAS layout synthesis system, and MOSFET devices, interconnect resistances and capacitances, and their locations extracted. Due to a problem with the LAS tool, we were only able to synthesize the six smallest benchmarks. Inputs to the sensitivity analysis were a set of critical paths, delay model, and extracted layout data. For each parameter variation, the variation in interconnect capacitances was calculated and used to calculate the path delay variation. Table II shows the statistics of our benchmark designs. Column 2 shows the number of interconnect nodes in the gate-level description. Columns 3-5 list the minimum, maximum, and average number of coupling capacitances per net. Note that in C432 one net couples to nearly half the other nets. Columns 6-8 list the minimum, maximum, and average number of critical coupled nets where the coupling capacitance is greater than 1%/5% of the total node capacitance. Even in these small benchmarks there are often a large number of significant coupling capacitances on each net. Table III and Table IV show the results of test generation under the AS and SS criteria, respectively. Column 2 shows the number of partial paths that are searched to build the set of 100 longest paths. The less constrained SIC of the SS criterion results in longer paths, but also results in many

more partial paths being considered in the search process. The CPU time in column 3 is measured on a Sun SPARC Ultra 1. Columns 4-6 show the averaged path delays relative to the best/worst-case UI at the primary output of each path by using three different delay calculation methods, and assuming nominal process parameters.

Table II. Statistics of ISCAS85 Benchmarks.

Ckt.	No. Nets	No. Cpld Nets			No. Crit. Cpld Nets (1%/5%)		
		Min.	Max.	Avg.	Min.	Max.	Avg.
C432	196	2	102	15	2/1	25/8	9/3
C499	243	1	84	12	1/1	22/8	7/3
C880	443	0	144	18	0/0	24/9	9/4
C1355	587	2	129	16	2/1	31/9	9/4
C1908	913	1	122	15	1/1	25/9	8/4
C2670	1502	2	187	28	1/0	29/8	10/3

Table III. 100 Longest Delay Paths (AS).

Ckt.	Partial Paths	CPU (sec)	Avg. PD in UI (%)			Longest PD (ps)		
			Gnd.	EPD	MEPD	Gnd.	EPD	MEPD
C432	4213	213	45.3	46.4	52.5	3465	3481	3641
C499	6699	287	45.2	45.5	50.3	3190	3337	3638
C880	8767	201	46.9	48.8	57.8	3878	3996	4334
C1355	12765	488	44.1	43.6	45.7	4250	4251	4446
C1908	49870	2908	48.1	49.3	52.5	6290	6366	6616
C2670	8934	2011	41.1	42.4	51.6	6549	6610	7229

Table IV. 100 Longest Delay Paths (SS).

Ckt.	Partial Paths	CPU (sec)	Avg. PD in UI (%)			Longest PD (ps)		
			Gnd.	EPD	MEPD	Gnd.	EPD	MEPD
C432	4412	177	46.2	47.4	50.6	4599	4632	4714
C499	4988	334	42.9	43.9	45.3	3500	3517	3705
C880	2805	89	47.5	48.9	63.7	4142	4228	4814
C1355	12094	645	44.2	45.2	47.6	4234	4251	4446
C1908	39238	2500	48.1	49.1	52.1	6411	6416	6620
C2670	45092	3894	43.0	43.0	55.1	6700	6707	7401

Column 4 (Gnd.) is the delay calculated using a grounded capacitor model. Column 5 shows the expected path delay (EPD) calculated using the ECCF model without searching for the worst-case couplings and treating the free nodes (S_{j11}, S_{j12}, and S_{j13} in Table I) as capacitors to ground. Column 6 shows the maximum expected path delay (MEPD) calculated using the ECCF model and searching for the worst-case couplings. There is little difference between columns 4 and 5, both being near the midpoint of the UI. The reason is that coupled node transitions are almost as likely to be helpers as aggressors when they are necessary for path sensitization. It is only when they are maximized in column 6 that there is a significant 5-10% delay increase. Actual delay values are shown in columns 7-9. The longest delay with the SS criterion is always larger than that with AS since SS is a superset of AS.

Figure 5 shows the upper bound (UB), lower bound (LB), EPD delay (EDLY), MEPD delay (MEDLY), and SPICE results for the 100 longest paths in circuit C2670 using the AS criterion. The upper and lower bounds are computed assuming every logic stage on the path is at their maximum or minimum delay, ignoring sensitization constraints. As can be seen, the MEDLY is a fairly good bound for the SPICE delay. In some cases the SPICE results diverge because the transition propagates down a different path, due to inaccuracies in the side input delay modeling and the ECCF model. In almost every case where a different path than the target is sensitized, the result is a shorter delay. The exception is a few paths in C499 and C1355 where the SPICE path is slightly longer than the predicted path. This can be corrected by using a slightly larger UI in the delay models. In C1908 there are 4 paths with SPICE delays significantly longer than our predicted delay for the target path. The actual sensitized paths are much longer than the target paths. Using the SS criterion avoids this problem.

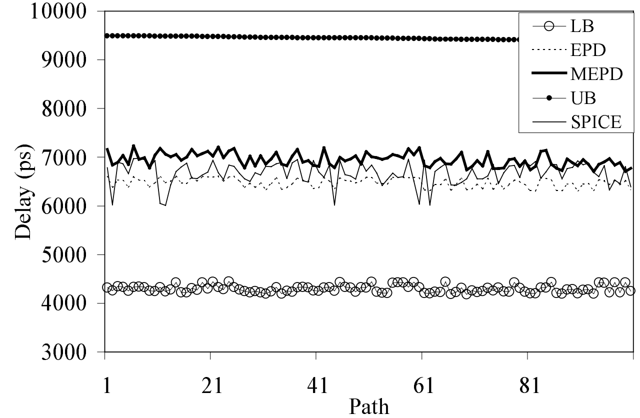

Figure 5. Predicted and SPICE Path Delays in C2670.

Table V shows the statistical timing analysis results. The +/-3σ and average percentage change and absolute values of the MEPD are shown for the 100 longest paths in each circuit. Interconnect process parameter variation causes a 5-10% delay variation. Table VI shows minimum, maximum, and average contribution of gradient and random spatial process parameter variation to delay variation. The gradient accounts for two-thirds of the variation, since on long paths random variations tend to cancel out [19]. Table VII shows the delay variation due to metal width (W), thickness (T), and ILD thickness variation.. Each circuit has a different sensitivity.

Figure 6 shows the delay variation of the 100 longest AS paths in C2670 including process variation. The process-based delay largely tracks across paths, and is more significant than the coupling-based variation. It is also much smaller than the upper and lower delay bounds.

6. Conclusions and Future Work

We have developed a statistical timing analyzer that takes into account capacitive coupling and process variation to estimate worst-case path delays. A model for interconnect coupling capacitance was built and the set of critical paths and input vectors determined for the worst case capacitive couplings. We developed and applied formulas to compute path delay variation due to process variation. In the future we plan to refine our approach so

that it can be used for delay test generation and delay fault simulation. In particular we will include gate delay variation, side path variation, and tracking of transitions. We also plan on combining this approach with local delay faults to build a general framework for ATPG, fault simulation and diagnosis of realistic delay defects.

Table V. Path Delay Variation due to Process

Ckt.	Min. 3σ Dly. Chng.		Max. 3σ Dly. Chng.		Avg. 3σ Dly. Chng.	
	Pct. (%)	Dly. (ps)	Pct. (%)	Dly. (ps)	Pct. (%)	Dly. (ps)
C432	5.4	195	10.9	389	7.8	279
C499	3.3	103	11.8	426	7.8	247
C880	6.7	249	13.2	497	8.6	334
C1355	6.2	227	11.2	500	8.5	329
C1908	7.8	487	11.9	743	9.3	586
C2670	5.5	394	11.2	793	8.0	556

Table VI. Path Delay Variation by Variation Type.

Ckt	Gradient Variation (%)			Random Variation (%)		
	Min.	Max.	Avg.	Min.	Max.	Avg.
C432	45.0	83.6	68.8	16.4	55.1	31.2
C499	54.1	83.2	71.8	16.8	45.9	28.2
C880	48.4	83.6	69.6	16.4	51.6	30.4
C1355	47.8	84.5	68.8	15.5	52.2	31.2
C1908	61.0	86.5	73.6	13.5	39.1	26.4
C2670	46.8	86.7	72.7	13.3	53.2	27.3

Table VII. Path Delay Variation by Process Parameter.

Ckt.	Delay Change Caused by Variation of Process Parameter (%)								
	M1W	M2W	M3W	M1T	M2T	M3T	ILD1	ILD2	ILD3
C432	0.6	4.7	7.5	14.1	13.0	25.7	0.0	18.4	15.8
C499	0.0	6.6	0.0	0.1	4.5	2.7	12.5	53.6	20.0
C880	0.0	3.0	5.8	3.1	4.6	8.9	13.2	44.9	16.6
C1355	5.1	4.9	5.2	6.4	5.2	5.2	8.6	40.0	19.5
C1908	7.6	10.8	2.8	23.5	25.0	10.0	0.9	17.4	2.0
C2670	24.8	11.3	9.6	31.7	14.4	5.9	0.3	1.3	0.7

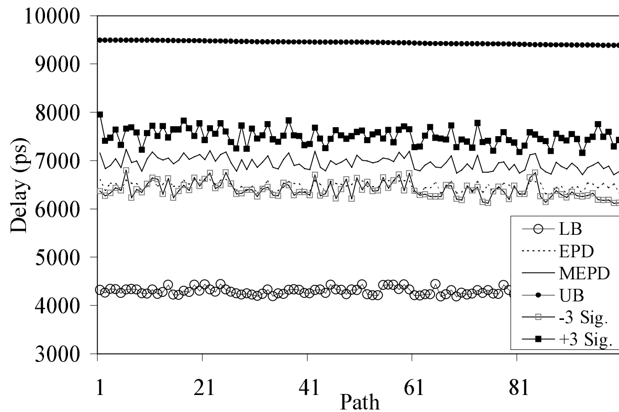

Figure 6. 3σ Path Delay Variation of C2670.

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