A Circuit Level Fault Model for Resistive Opens and Bridges

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Abstract

Delay faults are an increasingly important test challenge. Traditional open and bridge fault models are incomplete because only the functional fault or a subset of delay fault are modeled. In this paper, we propose a circuit level model for resistive open and bridge faults. All possible fault behaviors are illustrated and a general resistive bridge delay calculation method is proposed. The new models are practical and easy to use. Fault simulation results show that the new models help the delay test to catch more bridge faults.

1. Introduction

Delay testing detects small manufacturing defects that do not cause functional failure but affect the speed of integrated circuits.

Since modern VLSI circuits are interconnect dominant, this paper focuses on spot defects in the interconnect. There are two types of spot defects—opens and bridges. Previous research classified opens into strong opens (>10MΩ) and weak opens (≤10MΩ) [1]. Strong opens cause stuck-at faults and therefore, can be detected by regular stuck-at patterns. Weak opens cause delay faults and therefore, may not be detected by regular stuck-at patterns [2][3]. Rodriguez-Montanes and Gyvez showed that in modern deep sub-micron technology, the percentage of weak opens is high enough to require delay fault testing [1].

Previous bridge fault models include functional fault models and delay fault models. Chakravarty [4] showed that the path-delay fault model is not adequate to model the bridge fault. Sar-Dessai [5] gave several functional fault models for resistive bridge faults. Hao and McCluskey [6] studied the effect of bridge faults inside of logic gates. Moore [2] presented comprehensive delay fault analysis for resistive bridge models and coupling effects, but the delay calculation was not given. Renovell [7][8] presented detailed electrical behaviors for zero bridges and resistive bridges. Other techniques, such as the mixed-mode simulation method by Chuang [9] and neural network techniques by Shaw [10], give more accurate bridge fault models. But these methods are not efficient for large circuits due to their high time complexity. Vierhaus [11] used IDDQ test to detect the bridge fault. However, as the IC geometry scales down, IDDQ test becomes more difficult as the leakage currents increase.

In this paper we propose a physically realistic yet economical resistive open and bridge fault model to model delay faults as well as functional faults due to resistive opens and bridges. The fault model is reasonably accurate and easy to implement for fault simulation of large industrial circuits. We enumerate all possible fault behaviors and present the relationship between input patterns and output behaviors, which is useful in ATPG.

In this paper, the delay of a net is defined as the time between the input of the driver gate reaches 50% *Vdd* and the input of the downstream gate reaches 50% *Vdd*. An accurate yet simple delay calculation method is proposed. In this paper, we do not consider feedback bridges, bridge between nets feeding the same gate [5], inductive coupling, process variation, power supply and substrate noise [12]. We also assume two nets in a bridge fault are not feeding the same gate.

The remainder of the paper is organized as follows. Section 2 describes the resistive open model. Section 3 describes the resistive bridge model. Experimental results are included in each section. Section 4 concludes with discussions.

2. Resistive Open Fault Model

The resistive open fault model is shown in Figure 1. In this model, a resistive open is represented by a resistor r_o in a net at the location where the open defect may occur. The input buffer B1 and output buffer B2 represent arbitrary CMOS gates.

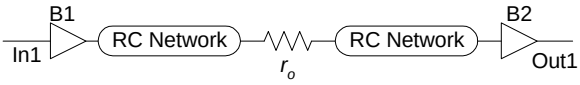

Figure 1. Resistive open fault model.

From extensive SPICE simulation, we found the delay increases almost linearly with the open resistance. Figure 2 shows the SPICE simulation result of a typical net using TSMC 250nm technology.

The open resistance is modeled as an increased delay *d'* in the net. The increased delay *d'* is approximated by a linear function $d' = r_o/R_{nominal} \cdot d$, where r_o is the open resistance, $R_{nominal}$ is the interconnect resistance without open and d is the nominal delay. Above a certain value,

depending on the clock frequency of the circuit the open becomes a stuck-open fault.

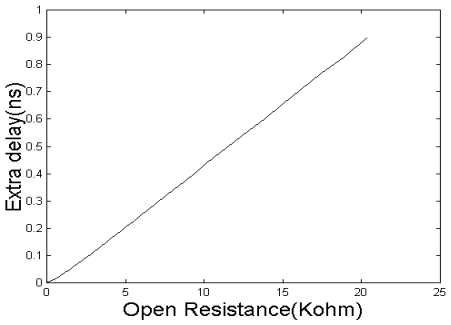

Figure 2. Delay increases linearly with open resistance.

3. Resistive Bridge Fault Model

The objective of the resistive bridge fault model is to transform the effect of a resistive bridge fault to a functional fault or a delay fault, and compute the extra delay caused by the bridge. We will first propose the circuit model, and then perform DC and transient analysis. Finally, we will give procedures to calculate the delay for the resistive bridge fault.

3.1. Circuit Model

The resistive bridge fault model is shown in Figure 3.

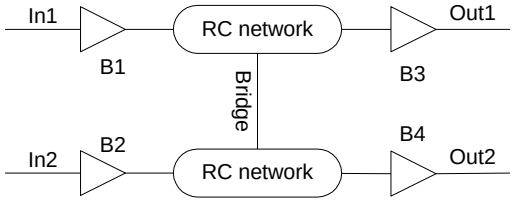

Figure 3. Resistive bridge fault model.

Each buffer can be an arbitrary CMOS gate. To simplify the analysis, CMOS devices in B1 to B4 are replaced by switches and linear resistors in Figure 4. We use a simple *RC* interconnect model that lumps interconnect parasitic capacitance with the load capacitance.

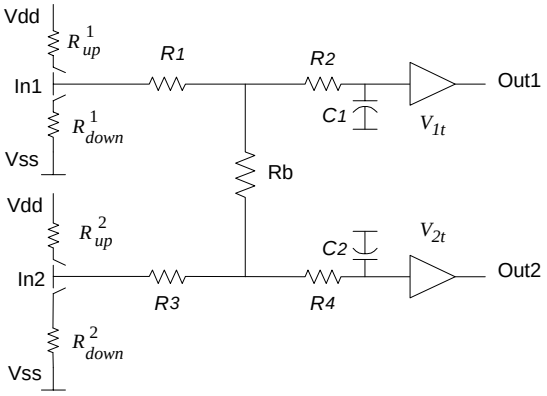

Figure 4. Simplified resistive bridge circuit model.

Circuit parameters in Figure 4 include pull-up and pull-down resistances R_{up}^1, R_{down}^1, R_{up}^2, and R_{down}^2 of B1 and B2, interconnect parasitic resistances R_1, R_2, R_3 and R_4, bridge resistance R_b, and logic interpretation voltages V_{1t}, V_{2t} of B3 and B4. The logic interpretation voltage V_t of a buffer is defined as follows. If the input of the buffer is below V_t, then the output will be low. If the input of the buffer is above V_t, then the output will be high.

3.2. DC Analysis

In DC analysis, it is assumed that input signals remain constant and output signals are stable. Therefore, all interconnect parasitic capacitances and sink capacitances are ignored.

There are four possible cases of input patterns in DC analysis. When In1 and In2 are both high, or both low, the bridge has no impact on the circuit. When In1 is low and In2 is high, the circuit is shown in Figure 5.

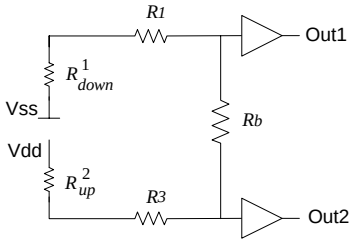

Figure 5. Circuit model when In1 is low and In2 is high.

Define the Bridge Threshold Resistance (BTR) for Out1 as

$$R_{1,Vss} = \frac{Vdd(R_1 + R_{down}^1)}{V_{1t}} - (R_1 + R_3 + R_{down}^1 + R_{up}^2). \quad (1)$$

When $R_b < R_{1,Vss}$, Out1 is high, which is a functional fault. When $R_b > R_{1,Vss}$, there will be no functional fault, but there might be an increaed delay, which is discussed in the next section. The relationship between output Out1 and R_b is illustrated in Figure 6.

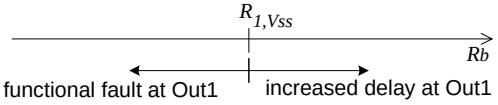

Figure 6. Relationship between R_b and Out1.

Similarly for Out2, the BTR is

$$R_{2,Vdd} = \frac{V_{2t}(R_3 + R_{up}^2)}{Vdd - V_{2t}} - (R_1 + R_{down}^1). \quad (2)$$

The case when In1 is high and In2 is low is symmetric. The corresponding BTRs are given as follows.

$$R_{1,Vdd} = \frac{V_{1t}(R_1 + R_{up}^1)}{Vdd - V_{1t}} - (R_3 + R_{down}^2), \quad (3)$$

$$R_{2,Vss} = \frac{Vdd(R_3 + R_{down}^2)}{V_{2t}} - (R_1 + R_3 + R_{down}^2 + R_{up}^1). \quad (4)$$

It is known that for Boolean functions with two inputs, only four are monotone and non-constant. Therefore, the behavior of Out1 in Figure 4 can only be one of the four in Figure 7. Table I summarizes the above analysis that tells us which model the circuit will behave.

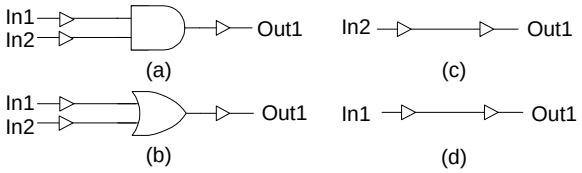

Figure 7. Four basic resistive bridge fault models for DC analysis.

Table I. Bridge fault model for Out1.

		Out1 Model
R_b range	$R_b \le \min(R_{1,Vdd}, R_{1,Vss})$	(c)
	$R_{1,Vss} < R_b < R_{1,Vdd}$ (if $R_{1,Vss} < R_{1,Vdd}$)	(a)
	$R_{1,Vdd} < R_b < R_{1,Vss}$ (if $R_{1,Vdd} < R_{1,Vss}$)	(b)
	$R_b \ge \max(R_{1,Vdd}, R_{1,Vss})$	(d)

Some useful properties can be derived directly from the models. For example, from equations (1) to (4), all BTRs cannot be greater than zero and lesss than zero at the same time. Thus, Out1 and Out2 cannot behave as Figure 7(c) simultaneously, i.e. the values cannot be swapped. When R_b=0, Out1 and Out2 cannot behave as Figure 7(d) simultaneously, i.e. there must be a functional fault at either Out1 or Out2.

3.3. Transient Analysis

In transient analysis, there are four types of input signals: high, low, rising (from low to high), and falling (from high to low). Using the results of DC analysis, we know that the output behavior will eventually settle down to one of the four fault models in Figure 7, determined by the BTR values. There are a total of 16 cases of input type combinations for In1 and In2. The analysis for all cases is similar to the following case.

Consider the case when In1 is rising and In2 is low. If $R_b \le R_{1,Vdd}$, the DC analysis shows that the circuit contains a functional fault for Out1 and can be detected by functional tests. If $R_b > R_{1,Vdd}$, there is no functional fault. The circuit model in Figure 4 can be simplified to the model in Figure 8.

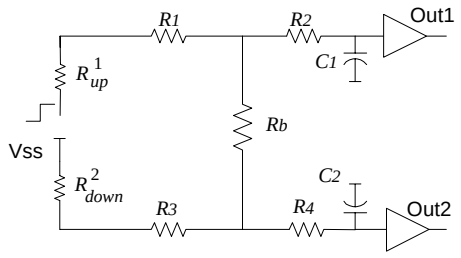

Figure 8. Circuit model when In1 is rising and In2 is low.

From SPICE simulation and circuit analysis with moment matching [13], we found that if there is a rising input on In1, the behavior of output Out1 can be approximated by the model shown in Figure 9.

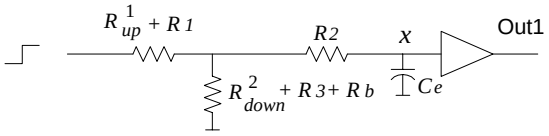

Figure 9. Approximation circuit model for Out1 when In1 is rising and In2 is low.

In Figure 9,

$$C_e = C_1 + \frac{(R^2_{down}+R_3)^2}{(R^2_{down}+R_3+R_b)^2}\,\frac{C_2}{1+\left|R_4-R_2\right|/(R^1_{up}+R_1+R_2)}.$$

Since the peak voltage of node *x* in Figure 9 is only a fraction of *Vdd*, there will be increased delay at Out1. Assuming the delay at Out1 without bridge is d_1, then the increased delay d' can be computed as

$$d' = (-b\cdot\frac{C_e}{C_1}\cdot\log_2(0.5\cdot(1-\frac{R^1_{up}+R_1}{R_b+R^2_{down}+R_3}))-1)\cdot d_1,$$

where

$$b = \frac{R_2}{R^1_{up}+R_1+R_2} + \frac{(R_1+R^1_{up})(R^2_{down}+R_3+R_b)}{(R^1_{up}+R_1+R_2)(R_b+R_1+R_3+R^1_{up}+R^2_{down})}.$$

The equation is derived analytically from the model in Figure 9 assuming a step input. SPICE simulation shows that it is also a good approximation for an input with a small slope.

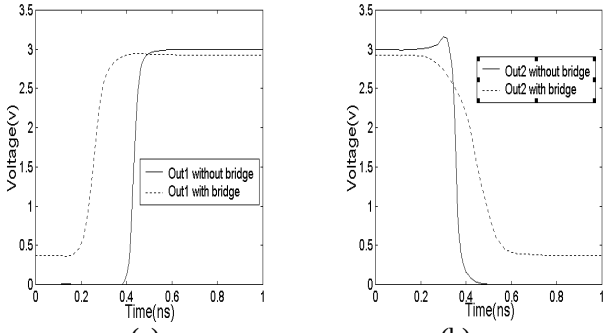

Figure 10. A bridge resistance causes decreased delay at Out1 (a) and increased delay at Out2 (b).

The bridge resistance can increase or decrease the delay [2] (d' can be greater or less than zero) depending on the input patterns. Figure 10 is the SPICE simulation of two interconnect segments from the layout of C432 of ISCAS85 circuit. In1 is rising, and In2 is falling, and both change simultaneously. The bridge resistance is 500Ω. There is a decreased delay at Out1, and an increased delay at Out2. The decreased delay may cause a hold time

violation or a race at Out1. This type of fault cannot be detected by the current delay fault testing.

3.4. Modeling Procedure

Based on the above analysis, we derive the bridge fault model as follows. All functional and delay faults are included in the model. Previous fault models such as the aggressor-victim models [2] are special cases of this model.

1. Compute R^1_{up}, R^1_{down}, R^2_{up}, R^2_{down}, V_{1t} and V_{2t} from the cell library. Compute R_1, R_2, R_3, R_4, C_1 and C_2 from the interconnect parasitics.
2. Compute BTR values $R_{1,Vdd}$, $R_{1,Vss}$, $R_{2,Vdd}$ and $R_{2,Vss}$ according to (1) to (4).
3. For fault simulation, we are given R_b. Use R_b to choose a fault model from Figure 11 according to Table I. Compute d' where

$$d' = (-c \cdot \log_2((0.5-h)/(g-h)) - 1) \cdot d_1, \quad (5)$$

d_1 is the nominal delay of Out1, c, g and h are chosen according to Table II.

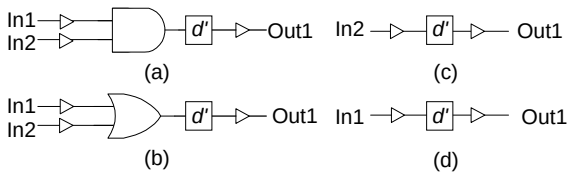

Figure 11. Four basic resistive bridge fault models.

Table II. Increased delay(ID) or decreased delay (DD) at Out1 for Figure 11(d), r means rising, f means falling, 1 means high, 0 means low, and other variables are defined in equation series (6).

Input Pattern(In1, In2)	Out1 behavior for Figure 11(d)
Both static (*0*, *0*) , (*0*, *1*), (*1*, *0*), (*1*, *1*)	No ID nor DD
Same direction (*r*, *r*), (*f*, *f*)	
In1 static (*0*, *r*), (*0*, *f*), (*1*, *r*), (*1*, *f*)	
(*r*, *0*)	*ID, g=0, h=m_1, c=$a_1.b_1$*
(*f*, *0*)	*DD, g=m_1, h=0, c=$a_1.b_1$*
(*r*, *f*)	*ID or DD, g=1–m_2, h=m_1, c= $a_1.b_1$*
(*f*, *r*)	*ID or DD, g=m_1, h=1–m_2, c= $a_2.b_2$*
(*r*, *1*)	*DD, g=1–m_2, h=1, c= $a_2.b_2$*
(*f*, *1*)	*ID, g=1, h=1–m_2, c= $a_2.b_2$*

In Table II, if both In1 and In2 change, it is assumed that the two signals change simultaneously. If the signals do not change at the same time, we treat the case as the combination of two cases happening sequentially. For example, if both inputs are rising and In1 is faster, then this case is consistent with the combination of (*r*, *0*) and (*1*, *r)*.

Some constants in Table II are given as follows.

$$a_1 = 1 + \frac{(R^2_{down} + R_3)^2}{(R^2_{down} + R_3 + R_b)^2} \frac{C_2/C_1}{1 + |R_4 - R_2|/(R^1_{up} + R_1 + R_2)},$$

$$a_2 = 1 + \frac{(R^2_{up} + R_3)^2}{(R^2_{up} + R_3 + R_b)^2} \frac{C_2/C_1}{1 + |R_4 - R_2|/(R^1_{down} + R_1 + R_2)},$$

$$b_1 = \frac{R_2}{R^1_{up} + R_1 + R_2} + \frac{(R_1 + R^1_{up})(R^2_{down} + R_3 + R_b)}{(R^1_{up} + R_1 + R_2)(R_b + R_1 + R_3 + R^1_{up} + R^2_{down})},$$

$$b_2 = \frac{R_2}{R^1_{down} + R_1 + R_2} + \frac{(R_1 + R^1_{down})(R^2_{up} + R_3 + R_b)}{(R^1_{down} + R_1 + R_2)(R_b + R_1 + R_3 + R^1_{down} + R^2_{up})},$$

$$m_1 = (R_b + R_3 + R^2_{down})/(R_b + R_1 + R_3 + R^1_{up} + R^2_{down}), \quad (6)$$

$$m_2 = (R_b + R_3 + R^2_{up})/(R_b + R_1 + R_3 + R^1_{down} + R^2_{up}).$$

For other models in Figure 11, the same delay formulas can be used to compute the increased delay or decreased delay, unless the input patterns causes functional faults at Out1.

Similar results for Out2 can be easily derived from Figure 11 and Table II by substituting Out2 for Out1, input pattern (In2, In1) for (In1, In2), $R_{2,Vdd}$ for $R_{1,Vdd}$ and $R_{2,Vss}$ for $R_{1,Vss}$. All the equations in (5) and (6) need to be recomputed by exchanging all the superscript 1 with 2, R_3 with R_1 and R_4 with R_2.

In Table II, there are two input patterns, (*r*, *f*) and (*f*, *r*), that may cause increased delay or decreased delay at Out1 and Out2 simultaneously. However, it can be derived from equation series (5) and (6) that the delay of Out1 with input (*r*, *0*) is greater than the delay with input(*r*, *f*), and the delay with input (*f*, *1*) is greater than the delay with input (*f*, *r*). Therefore, to maximize the delay at Out1, the best input patterns are (*r*, *0*) and (*f*, *1*), in which it is hard to compare the former with the later. To maximize the delay at Out2, the best input patterns are (*0*, *r*) and (*1*, *f*). Similarly, to minimize the delay at Out1, the best input patterns are (*r*, *1*) and (*f*, *0*) and to minimize the delay at Out2, the best input patterns are (*1*, *r*) and (*0*, *f*). To maximize or minimize the delay at both output simultaneously, the best input patterns may be (*r*, *f*) and (*f*, *r*).

For cases (*r*, *0*) and (*f*, *0*), simulation results of one example circuit are shown in Figure 12 and Figure 13. We use TSMC 250nm 3V technology. Each net contains two buffers and each buffer at input and output use two identical inverters. The PMOS size of the inverter (width/length) is 9.6u/0.3u, and NMOS size is 4.8u/0.3u. The logic interpretation voltage is 1.3V. The bridge locates between the middle of the two nets. BTRs $R_{1,Vdd}$ for Out1 is greater than zero and $R_{1,Vss}$ is less than zero. Out1 can only behave as Figure 11(d) and (a) based on Table I.

When $R_b > R_{1,Vdd}$, in both Figure 12 and Figure 13, Out1 behaves as Figure 11(d) and an increased delay exists. Bridge defects falling in this range may be detected by

delay test with our fault model, but may not be detected by traditional functional fault test.

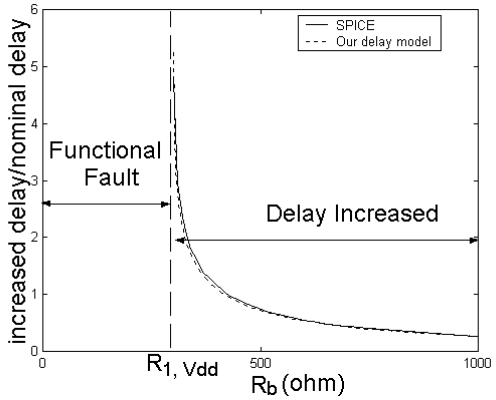

Figure 12. Example relationship between R_b and increased delay at Out1 for rising input.

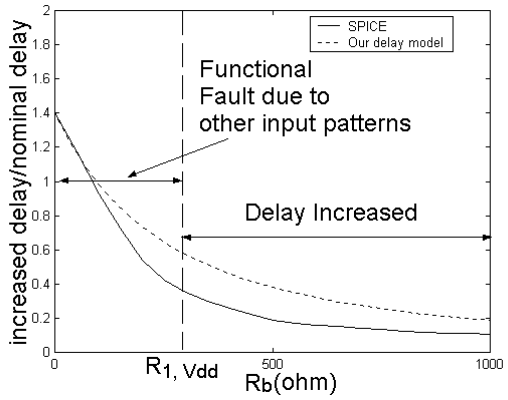

Figure 13. Example relationship between R_b and increased delay at Out1 for falling input.

When $R_b<R_{1, Vdd}$, Out1 behaves as Figure 11(a) in both figures but appears as a functional fault in Figure 12 and an increased delay in Figure 13. Simulation results show that when Out1 behaves as Figure 11(a) ($R_b<R_t$), even though there is a delay fault for Out1 under some input patterns, bridge defects in this range can still be tested by traditional functional test patterns. Both delay test and functional test may detect bridge defects.

Our model shows a good match with SPICE. The error is mainly caused by the approximation of effective capacitance from Figure 8 to Figure 9.

3.5. Effectiveness

Table III shows the percentage of bridges in the ISCAS85 circuits that cannot be detected by functional test but can be detected by delay fault test using our bridge fault model. The layout is done with Cadence Silicon Ensemble™ to TSMC 250nm 3V 3-metal technology. Commercial parasitic extraction tools are used to extract parasitics and compute net delays. The logic interpretation voltage is 1.3V, and pull-up/down resistances of all gates are from 200Ω to 4KΩ. The clock period is set to be 5% longer than the delay of the longest structural path.

Table III. Percentage of bridge faults that are delay faults.

Circuit	Total Bridges	Delay faults
c432	821	56.8%
c499	1,102	44.8%
c880	1,412	38.6%
c1355	2,488	34.1%
c1908	4,007	37.9%
c3540	8,919	27.8%
c5315	12,168	23.3%
c6288	14,170	35.8%
c7552	12,156	17.9%

In the experiment, bridge faults are generated at each location where a coupling capacitance exists in the layout. The bridge resistance is assumed uniformly distributed [14] from 0Ω to 40KΩ. For each bridge, let R_f be the maximum resistance value below which the fault can be detected by the functional test, and R_d be the maximum resistance value below which the fault can be detected by the delay test. Then the percentage of bridge faults that can be detected only by delay fault test is $(R_d–R_f)/R_d$ for this bridge. Averaging for all bridges, we have the percentage reported in the table. Circuit c2670 is not included due to a parasitic extraction tool problem.

4. Conclusions

In this work we described physically realistic resistive open and bridge fault models incorporating both functional and delay effects of spot defects. For resistive opens, we show that the extra delay increases linearly with the open resistance. For resistive bridges, we first derive thresholds (BTR) for functional and delay faults, then propose a closed form delay calculation method for bridge faults. Experimental results show our delay calculation is accurate and efficient.

Our effective analysis results show that bridge fault models we proposed do help to test more delay faults caused by bridge defects. The new fault model and the fault coverage metric will be implemented in a later tool.

Acknowledgements

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