Comparison of Effectiveness of Current Ratio and Delta-I_{DDQ} Tests

Sagar S. Sabade D. M. H. Walker
Department of Computer Science
Texas A&M University
College Station, TX 77843-3112
Phone: (979) 862-9484
Fax: (979) 847-8578
E-mail: [sagars, walker]@cs.tamu.edu

Abstract

I_{DDQ} test is a valuable test method for semiconductor manufacturers. However, its effectiveness is reduced for deep sub-micron technology chips due to rising background leakage. Current two test methods that promise to extend the life of I_{DDQ} test are Current Ratio and Delta-I_{DDQ}. Although several studies have been reported on these methods, their effectiveness in detecting defects has not been contrasted. In this work, we compare these two methods using industrial test data.

1. Introduction

Higher chip performance is obtained by shrinking transistor geometries. However, as transistors become smaller, it is necessary to scale the supply voltage as well as the threshold voltage [1]. This results in the exponential increase in the leakage current (I_{DDQ}) [2]. Moreover, increased process variations cause large inter-die variation in I_{DDQ}. This makes distinguishing faulty and fault-free currents difficult. I_{DDQ} testing loses its effectiveness with rising background currents in Deep Sub-micron (DSM) chips [3] as it is highly difficult to separate flawed or outlier chips from fault-free chips [4]. Researchers have proposed different alternatives to resolve this issue and extend the usability of I_{DDQ} test to the DSM era [5]. Two most promising techniques used in industry today are the Current Ratio (CR) [6] and Delta-I_{DDQ} methods [7]. Both of these methods have their distinct merits and limitations. However, to our knowledge no work so far has contrasted these methods. What is the defect sensitivity of CR and delta I_{DDQ}? How does CR and delta change with different vectors? In this paper, we attempt to find answers to such questions using industrial test data[1]. It is understood that some answers cannot be generalized, but this analysis is helpful to understand the general trend.

The remainder of the paper is organized as follows. In the next section, we describe the basic concept of delta-I_{DDQ}. Section 3 describes the basic theme of current ratios (CR). Section 4 includes analysis results that compare CR and delta-I_{DDQ} tests using empirical test data. Section 5 shows vector sensitivity analysis of CR and delta-I_{DDQ}. Section 6 concludes the paper.

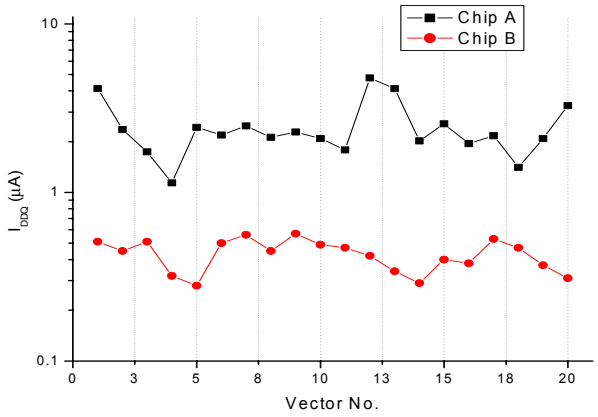

Figure 1. I_{DDQ} readings for two chips.

2. Delta-I_{DDQ}

The variability in fault-free leakage current primarily occurs due to two reasons: (1) vector-to-vector variation due to circuit topology as leakage current takes different paths and, (2) variation in transistor geometries due to process fluctuations. Delta-I_{DDQ} relies on the premise that within-chip variation in fault-free leakage current is smaller than that caused by the defective current. In this method, differences (deltas) in I_{DDQ} readings for consecutive vectors for a chip are obtained. That is, delta-I_{DDQ} is given by:

$$\Delta I_{DDQ(i)} = I_{DDQ(i)} - I_{DDQ(i-1)} \qquad (1)$$

where $I_{DDQ(i)}$ ($I_{DDQ(i-1)}$) is the I_{DDQ} value for the i^{th} ((i-1)th) vector. Due to random variations in I_{DDQ}, some deltas are positive and some are negative. Hence, for a fault-free chip, the mean delta ($\triangle\mu$) is expected to be zero and the variance is expected to be small. In general, since all deltas do not cancel out completely, the mean is a small nonzero value. For a defective chip, even if a single vector excites the defect, delta is considerably larger than other deltas. This results in greater variance and higher nonzero mean. Thus, it is possible to distinguish between faulty and fault-free

[1]This data comes from IBM/SEMATECH and LSI Logic. The conclusions drawn are our own and do not represent the views of these companies.

ICs using mean and standard deviation (SD).

Fig. 1 shows I_{DDQ} readings for two chips for twenty different vectors. Both chips passed all functional tests. However, there is up to an order of magnitude difference in the *corresponding* I_{DDQ} readings. Both chips also exhibit different vector-to-vector variation. This illustrates the difficulty in determining a single "justifiable" pass/fail limit. The histograms of delta-I_{DDQ} for these chips are shown in Fig. 2. Notice that the mean and SD of chip B (μ=0.0042,σ=0.1) is ten times smaller than that for the chip A (μ=0.045,σ=1.12). This illustrates that selecting a pass/fail threshold for delta I_{DDQ} is difficult.

2.1 Delta-I_{DDQ} Variations

Several variations of delta-I_{DDQ} have been reported in the literature. Instead of taking differences in the consecutive readings, difference in all I_{DDQ} readings with respect to the first I_{DDQ} reading is suggested. In this method, the first measurement is taken and a guard band is set around it. If any later I_{DDQ} measurement falls outside this guard band, the chip is rejected [8]. This method is useful for production implementation as only the comparison with a single I_{DDQ} threshold is required and it simplifies the tester instrumentation. Another delta-I_{DDQ} method is to use the difference between the maximum and minimum I_{DDQ} for screening (min-max method).

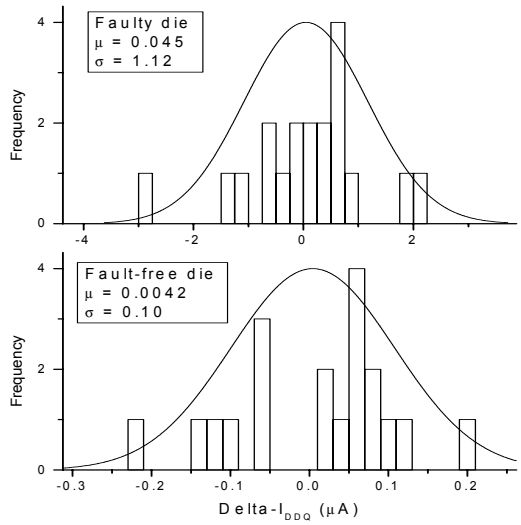

Figure 2. Delta-I_{DDQ} histograms.

In the delta-I_{DDQ} technique mentioned so far the variable component is the input pattern (test vector). Similarly, delta-I_{DDQ} can be defined for I_{DDQ} readings measured at different temperatures [9], supply voltages and before and after burn-in [10]. The properties of each fault-free delta-I_{DDQ} signature are different. For example, I_{DDQ} at higher temperature is higher than that at lower temperature. Thus, the mean value of fault-free delta-I_{DDQ} is non-zero. In general defect current does not change appreciably with temperature. Hence for a defective chip for a vector that excites the defect temperature-based delta-I_{DDQ} is negative. The temperature-based method is not desirable in a production test environment due to cost. Although delta-I_{DDQ} is predicted to lose its defect screening resolution for future technologies [11], it still remains a popular test.

3. Current Ratios

A fault-free chip that leaks more should consume proportionately high current for *all* input patterns. On the other hand, a chip having an active (pattern-dependent) defect consumes high current only when the defect is excited. In this case, the leakage current depends on the nature and resistance of the defect, among other parameters. Maxwell *et al*. observed that in spite of an order of magnitude difference in I_{DDQ} values, two dice had similar current signatures as shown in Fig. 3 [12]. Hence, it was proposed that ratios of the maximum I_{DDQ} to the minimum I_{DDQ} for fault-free chips would have small variation and can be used as a pass/fail criterion. The signature was described using an equation of the form:

$$\text{Max } I_{DDQ} = \text{Slope} \cdot \text{Min } I_{DDQ} + \text{Intercept} \qquad (2)$$

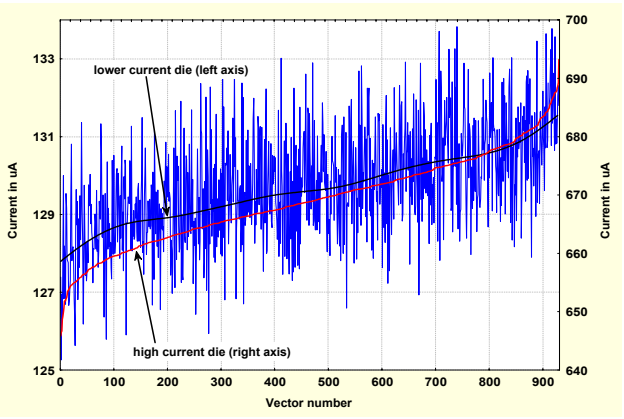

Figure 3. Fault-free chips have different I_{DDQ} magnitude but similar CRs.

Thus, the maximum I_{DDQ} was described as a function of minimum I_{DDQ} value. The authors characterized a sample of chips and determined CRs for several fault-free chips. Through linear regression they determined the parameters (the slope and the intercept) of the equation shown above. To account for unmodeled process variations, a guard band was added. In production, I_{DDQ} was measured for all vectors, CR was computed and a chip was rejected if its CR exceeded the threshold value.

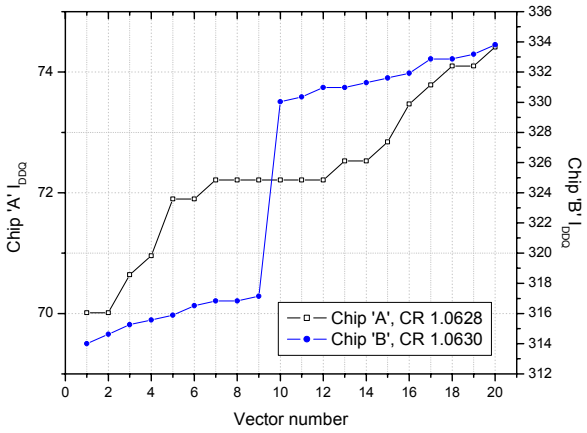

Figure 4. Similar CRs does not necessarily imply fault-free chips; A defective chip ('B') has CR similar to fault-free chip 'A'.

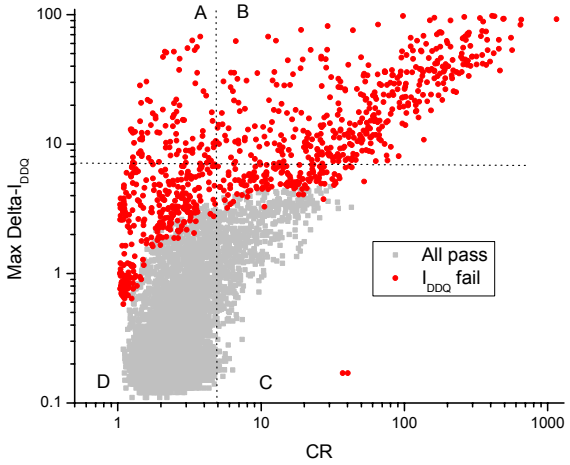

Figure 5. CR/delta-I_{DDQ} scatter plot for IBM data.

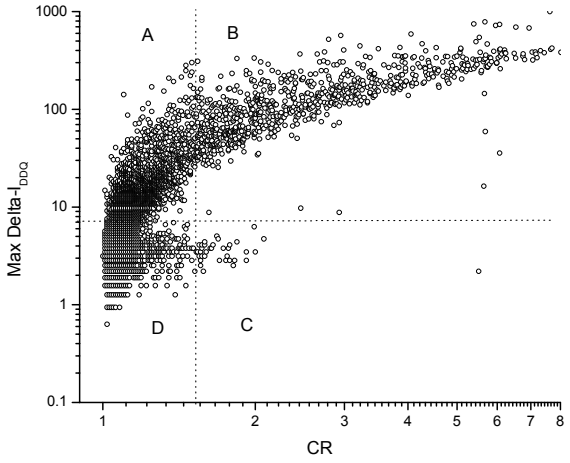

Figure 6. CR/delta-I_{DDQ} scatter plot for LSI data.

However, similar CRs do not necessarily mean that both chips are fault-free. This is illustrated with the help of Fig. 4. It shows current signatures for two dice from a wafer having different I_{DDQ} currents, but similar CRs. Chip B clearly has an active defect as indicated by a step of 15 units.

4. Analysis Results

In this section, we use production test data from IBM/SEMATECH and LSI Logic for comparing ΔI_{DDQ} and CR. The information about the data is included in the Appendix. We obtained CRs for all chips and delta-I_{DDQ} for two consecutive vectors. The scatter plot for CR and maximum delta I_{DDQ} for IBM data is shown in Fig. 5. It is divided into four quadrants using CR and delta-I_{DDQ} thresholds obtained from a data sample. Chips in quadrant 'B' are obvious outliers for which both CR and delta I_{DDQ} are high. These chips contain active defects. In quadrant 'D', both CR and delta I_{DDQ} are in agreement. These chips are either fault-free or have passive defect. Chips in quadrant 'A' have a passive or a subtle active defect that shows only moderate change in CR but correspondingly higher change in delta I_{DDQ}. For example, a chip with fault-free current range of 5 to 10 µA has a CR of 2 and delta I_{DDQ} of 5. In the presence of a passive defect that contributes 15 µA additional leakage, CR reduces to 1.25. The chips in quadrant 'C' have higher CR but smaller delta-I_{DDQ}. This occurs because of the specific order of vectors that results in small deltas. A similar scatter plot for LSI Logic data is shown in Fig. 6.

TABLE I. IBM data distribution for sample thresholds.

Wafer test	CR ≤ 5		CR > 5		BI test
	Δ ≤ 7	Δ > 7	Δ ≤ 7	Δ > 7	
All Pass	997	-	59	-	AP
	22	-	5	-	IF
	19	-	-	-	BF
	9708	-	453	-	NB
I_{DDQ} Fail	103	8	74	47	AP
	157	77	45	326	IF
	8	3	5	5	BF
	22	7	5	32	NB
BF: Boolean fail, NB: No BI					

We selected thresholds for CR and delta-I_{DDQ} from a randomly selected sample. To account for lot-to-lot variation in threshold selection, the sample is selected randomly from different wafers and lots. For IBM data, the threshold for CR is 5 and for delta-I_{DDQ} is 7. For LSI data the thresholds for CR and delta-I_{DDQ} are 1.7 and 7.7, respectively. Using these thresholds the distribution of data is as shown in Tables I and II. IBM data is subdivided using post burn-in (BI) test result. For LSI Logic data, BI test is not conducted.

If we compute the failure rate (percentage of chips failing Boolean test after burn-in) for each quadrant, for reasonable agreement on "good" and "gross outlier" chips (i.e. similar failure rates for quadrant B and D,

3.8 and 3.3%, respectively), the failure rate of quadrant A is higher (7.4%) than that for quadrant C (6.1%) showing delta-I_{DDQ} to be marginally more effective than CR for this dataset.

TABLE II. LSI data distribution for sample thresholds.

CR ≤ 1.7		CR > 1.7	
Δ ≤ 7.7	Δ > 7.7	Δ ≤ 7.7	Δ > 7.7
867593	72967	235	9451

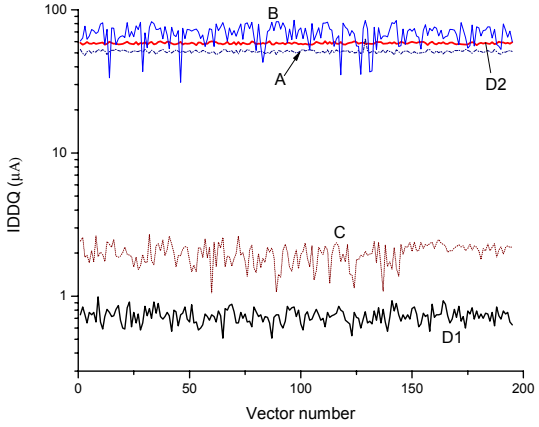

Figure 7. Sample IBM chips from each quadrant.

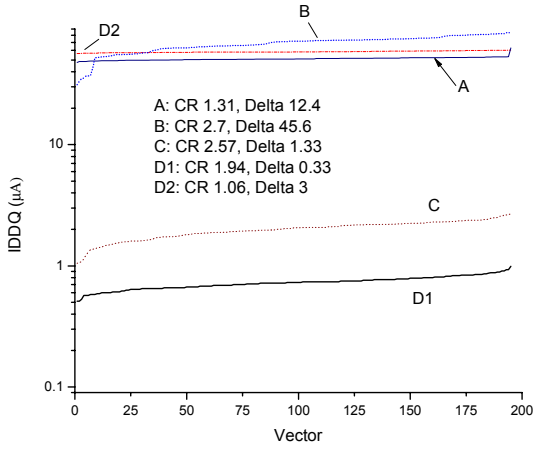

Figure 8. Current signatures for chips used in Fig. 7, maximum within-chip delta is shown.

4.1 Current Signatures for Sample Chips

We selected a sample of chips from each quadrant to verify our assumptions about defect types. Fig. 7 shows I_{DDQ} readings for a chip from each quadrant (A, B, C) and two chips (D1, D2) from quadrant D for IBM data. Fig. 8 shows the current signatures for these chips. Chip 'B' is an obvious outlier as indicated by the steps in the signature. Such chips can be detected by graphical signature analysis [13]. Chip 'A' has a passive defect and the chip 'C' has a subtle active defect (a small step is noticeable at the start of the signature). Both chips 'D1' and 'D2' are from the quadrant D. The chip 'D1' is a fault-free chip. The chip 'D2' has a combination of an active and a passive defect. However, the background leakage due to the passive defect is so high that the effect of the active defect on CR or delta I_{DDQ} is too small to be detected by the thresholds used. A similar behavior is also observed for the LSI data (see Fig. 9). The chip 'D' is fault-free, however, the presence of a subtle active defect in chip 'C' is not detected by the CR or delta-I_{DDQ} method. This underscores the fundamental limitations of CR and delta-I_{DDQ} methods in screening passive defects. It is possible to screen passive defects by using a lower bound on CR at the expense of rejecting some fault-free chips. However, as shown in the next section, such threshold setting is hard due to rapid fall of the CR distribution.

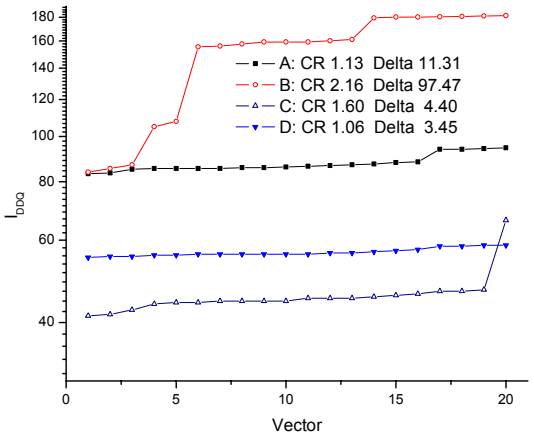

Figure 9. Current signatures for chips from LSI data.

5. Vector Sensitivity Analysis

The defect screening resolution of both CR and delta-I_{DDQ} depends on the number of vectors. The probability of detecting a defect increases with the number of vectors. In this section, we evaluate the vector sensitivity of both methods. Table III shows how CR and maximum delta I_{DDQ} (for two consecutive vectors) change with the number of vectors for a sample chip. The relative variation in delta I_{DDQ} is more than CR making it more sensitive to defects. Note however that vector ordering eventually decides sensitivity of delta I_{DDQ}.

I_{DDQ} can only be measured after internal circuit activity is settled down, thus making I_{DDQ} a slow test. Although some high-speed measurement methods like QuiC-Mon [14] have been developed, there is a strong motivation for reducing the number of test vectors without compromising the test quality. We observed the effect of selecting a pair of vectors such that one of them mostly yields the minimum I_{DDQ} and the other the maximum I_{DDQ} for a sample of chips. Fig. 10 shows the how many times each vector resulted in minimum or maximum I_{DDQ} for a smaller sample (from a wafer).

Vector #1 mostly results in the maximum I_{DDQ} and Vector #20 mostly results in the minimum I_{DDQ}. We then considered the entire data sample to observe the effect of vector pair selection on CR distributions. Fig. 11(a) shows the distribution of CR values when all 20 vectors are used. After using only vectors #1 and #20 for CR computation, the distribution of CRs for these chips (83580 chips, 118 wafers) is shown in Fig. 11(b). The shift in CR distribution is clearly visible. With more vectors higher CRs are obtained, thus shifting the distribution towards the right. As mentioned earlier, for passive defects CR actually reduces with increasing background leakage. When fewer vectors are used, the effect of random leakage around the constant value due to passive defects is either too small to be detected by CR or active defects are not excited by a given set of vectors. This becomes clearly visible in smaller CR range (1-1.20) shown in Fig. 12.

Table III. ΔI_{DDQ} and CR variation with vectors.

No. of vectors	Min I_{DDQ}	Max I_{DDQ}	Max ΔI_{DDQ}	CR
2	64.980	65.924	0.2151	1.0145
3			0.3144	
4		66.867	1.5721	1.0290
5				
6	64.666			1.0340
7				
8	64.352			1.0390
9		67.810	3.4586	1.0537
10				
11				
12				
13				
14				
15				
16				
17	63.094			1.0747
18				
19				
20				

6. Conclusions

With increasing background leakage current, I_{DDQ} testing becomes a difficult challenge. Methods such as CR and delta-I_{DDQ} extend the usability of I_{DDQ} test. In this work these two methods are compared for their effectiveness using industrial test data. Both the methods have the inherent limitation of not being able to screen passive defects. The increase in background leakage reduces CR and precludes the detection of passive defects. Setting a lower threshold on CR for detection of passive defects is difficult due to rapid fall of the distribution and accompanying yield loss. Since both these methods use intra-die variance analysis for defect detection, they will lose their defect screening resolution as vector-to-vector variation increases for DSM chips. CR will lose it faster than delta-I_{DDQ}. In general, methods that consider inter-die variance will be needed for survival of I_{DDQ} test for a few more technology nodes. Such methods include Nearest Neighborhood Residual (NNR) [15], Neighbor Current Ratio [16] and combination of them [17].

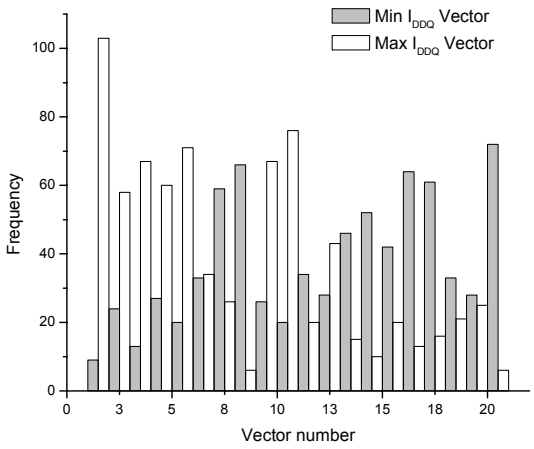

Figure 10. Distribution of min/max I_{DDQ} vectors for sample of chips (sample size 757 chips).

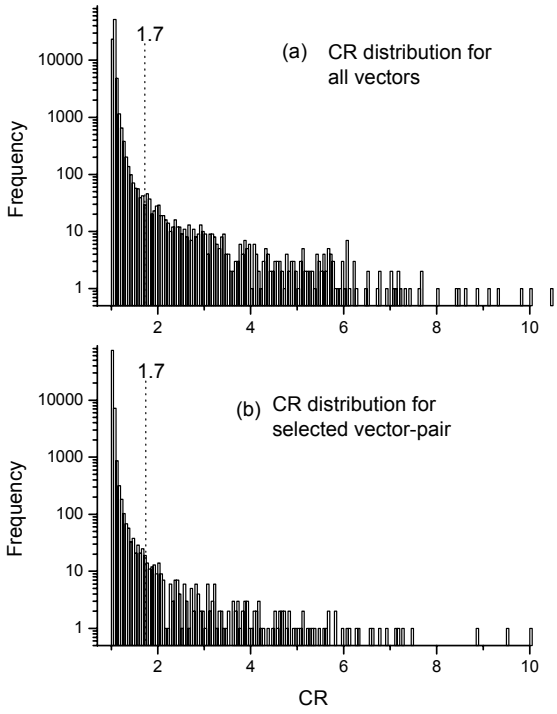

Figure 11. (a) Distribution of CR for all vectors and (b) after using only selected vector pair.

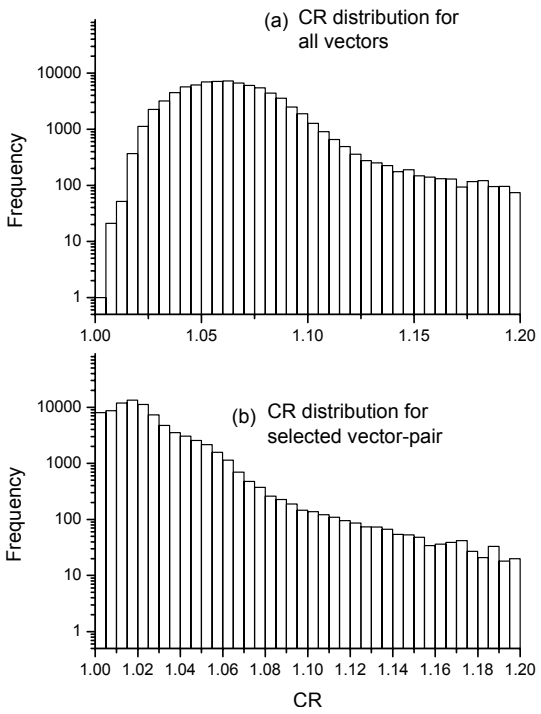

Figure 12. Change in CR distribution in the range 1-1.2 for all vectors and for selected vector pair.

Appendix

IBM/SEMATECH Data

This data comes from SEMATECH experiment S-121 for 0.6 μm technology. Data for 12570 chips is used. For each chip, a total of 195 I_{DDQ} measurements are available. Some chips passed all tests while some failed only delay test or the 5 μA threshold I_{DDQ} test (I_{DDQ} fail). A sample of chips underwent burn-in and all wafer-level tests were conducted after 6-hours of burn-in.

LSI Logic Data

The LSI test data comes from for 949753 chips from 1219 wafers and 79 lots for 180 nm technology. For each die on a wafer, 20 I_{DDQ} measurements are available. Due to the proprietary nature of the data, the I_{DDQ} pass/fail limit used by LSI Logic is unknown. Also for the same reason, the unit of measurement is not shown for LSI test data.

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