I_{DDX}-based Test Methods: A Survey*

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Abstract

Supply current measurement-based test is a valuable defect-based test method for semiconductor chips. Both static leakage current (I_{DDQ}) and transient current (I_{DDT}) based tests have capability of detecting unique defects that improves the fault detection capacity of a test suite. Collectively these test methods are known as I_{DDX} tests. However, due to advances in the semiconductor manufacturing process, the future of these test methods is uncertain. This paper presents a survey of the research reported in the literature to extend the use of I_{DDX} tests to deep sub-micron (DSM) technologies.

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1. INTRODUCTION

TESTING of Integrated Circuits (ICs) is a complex task. It becomes more challenging with increasing design complexities as integration density increases. Several methods are used to test ICs [1]. They can be broadly classified into two categories: operational tests and defect-based tests (DBT). The goal of operational tests is to verify the functionality of the chip. An example of this type is functional test. The DBTs target the physical *defects* using their abstract representation known as a *fault*. The absence of a defect (or inability to detect it) passes the test. Some tests, called structural tests, rely on the circuit structure for defect detection [2]. Such tests include stuck-at or scan test, delay test (AC scan), leakage current (I_{DDQ}), and transient (I_{DDT}) current test. AC scan and I_{DDQ}/I_{DDT} tests are also called parametric tests since they measure chip parameters like speed and current, respectively. Parametric tests have been used to improve the quality of shipped ICs [3]. Another example of parametric or specification test is Very Low Voltage (VLV) test that tests the device at a reduced voltage.

Functional test consists of applying predetermined patterns called *test vectors* at the inputs of an IC and comparing the behavior of the IC with the expected one. For example, a functional test for an adder may consist of applying the input patterns and examining the output for the correct result of addition.

A scan-based testing method is a structural test that checks combinational logic, flip-flops or latches and connectivity by placing the device in a logic state and changing it by shifting patterns through the flip-flops when they are configured into shift registers (*scan chains*). A mismatch in the output pattern indicates

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a defective device. The at-speed test applies patterns at the rated frequency of the device to verify whether it is capable of operating at the required speed. The AC scan delay test uses scan chains to deliver vector pairs that verify timing behavior on specific paths (path delay test) or on identified gates or connections that are represented as faults (transition delay test) [4]. In general, functional, structural, and parametric tests are complementary in nature and integral components of a test suite.

This paper presents an overview of current-based (I_{DDQ}/I_{DDT}) test methods, collectively known as I_{DDX} tests. The remainder of the paper is structured as follows. The next two sections explain the basic principle of static leakage current (I_{DDQ}) and transient current (I_{DDT}) tests. We then describe the advantages of I_{DDX} test. The challenges for I_{DDX} test are outlined in the following section. Then we provide a brief review of I_{DDQ} and I_{DDT} test methods. Finally, the paper concludes with some comments on future of I_{DDX} test for the state-of-the-art technologies.

2. PRINCIPLE OF I_{DDQ} TEST

Leakage current (I_{DDQ}) test [5][6] is a defect-based test that measures device supply current under steady state conditions. Fully static CMOS circuits consume little power when their inputs are stable [7]. This is because there is no direct path from the V_{DD} supply rail to ground. Hence if an IC draws a large amount of current when its inputs are stable, it is likely to be defective. This is the basic philosophy behind I_{DDQ} testing [8][9][10]. An I_{DDQ} test is capable of detecting shorts (bridges) between two switching nodes or a signal and power supply line (both categories referred to as an *active* or *pattern-dependent defect*) or between V_{DD} and ground (called a *passive or pattern-independent defect).* An active defect increases leakage for some (but not all) input patterns while a passive defect increases leakage for all input patterns. An active defect degrades functionality of a chip (due to reduced noise margin, etc.). For this reason, several I_{DDQ} test methods are targeted towards discarding chips with active defects. A passive defect may not affect the functionality, but increases the power consumption of a chip. It also reduces the reliability of a chip and can result in a customer return [11].

The basic theme of I_{DDQ} testing can be better explained with the help of an inverter circuit shown in Figure 1(a). In the absence of a defect and when the input is stable, the quiescent current flowing from V_{DD} to ground is low (since there is no direct path from V_{DD} to ground), as shown in Figure 1(b). In the presence of a defect (e. g. source-drain short, as shown in Figure 1(a)), however, significant current flows through the transistors. Thus, it is possible to identify a defective chip by measuring the elevated leakage current. Notice that several other bridging defects in the circuit (e. g. V_{DD}-to-ground short, gate-to-source short, inter-gate bridges, etc.) can also result in elevated I_{DDQ} [12]. Several other defects can be detected by I_{DDQ} test [13][14]. Since many advanced chips use static CMOS technology, I_{DDQ} is a valuable test method. It is observed that I_{DDQ} test forms an important component of a test suite for Deep Sub-Micron (DSM) technologies [15].

I_{DDQ} test differs from a functional test in that there is no inherent pass/fail condition. A chip consuming more current than the threshold ("I_{DDQ}-fail" chip) can still pass all functional tests. This poses a dilemma for semiconductor manufacturers as rejecting I_{DDQ}-only failed chips can result in unacceptable yield loss

[16][17]. On the other hand, a chip that consumes excessive current must contain some defect that was undetected by other tests (e. g. a highly resistive bridge). Such a chip can fail later in the system and result in a customer return in which case there are direct (replacement of the defective part) and indirect (manufacturer's reputation) costs associated with it [18]. This dilemma existed even before the emergence of DSM technology [19] as it complicates the test economics and the pass/fail threshold selection. Unfortunately, it worsens with each technology advancement.

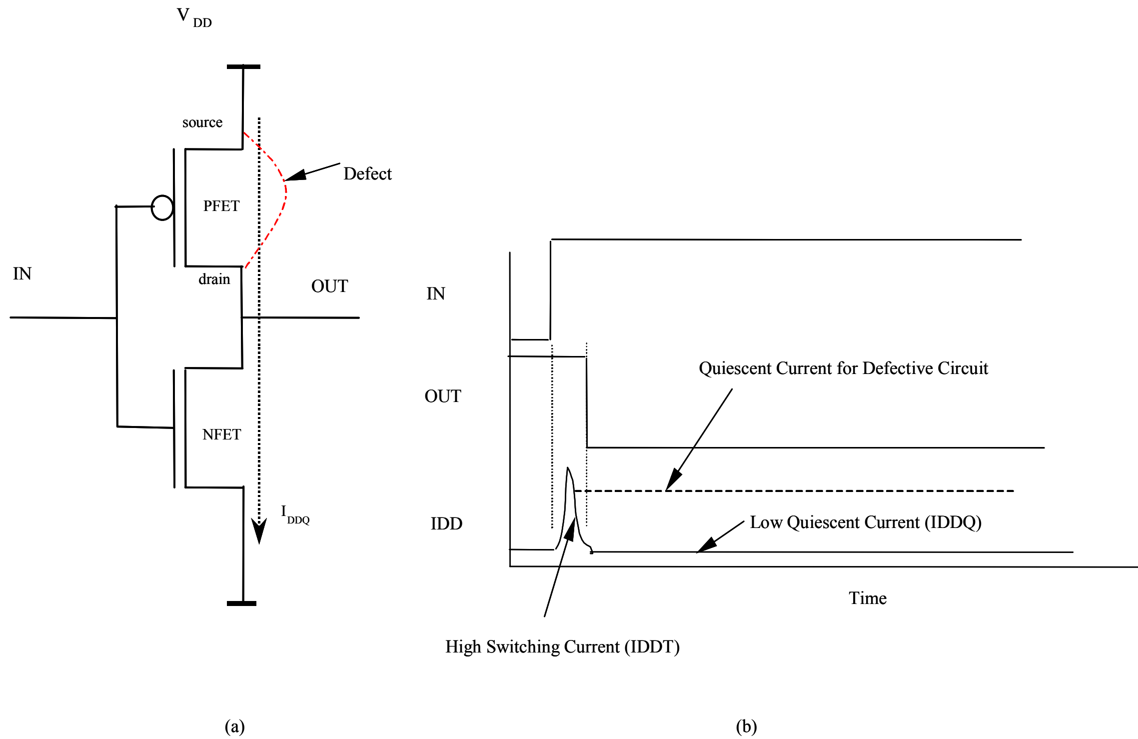

Fig. 1. (a) I_{DDQ} flowing through inverter is usually low, (b) but increases in the presence of a defect .

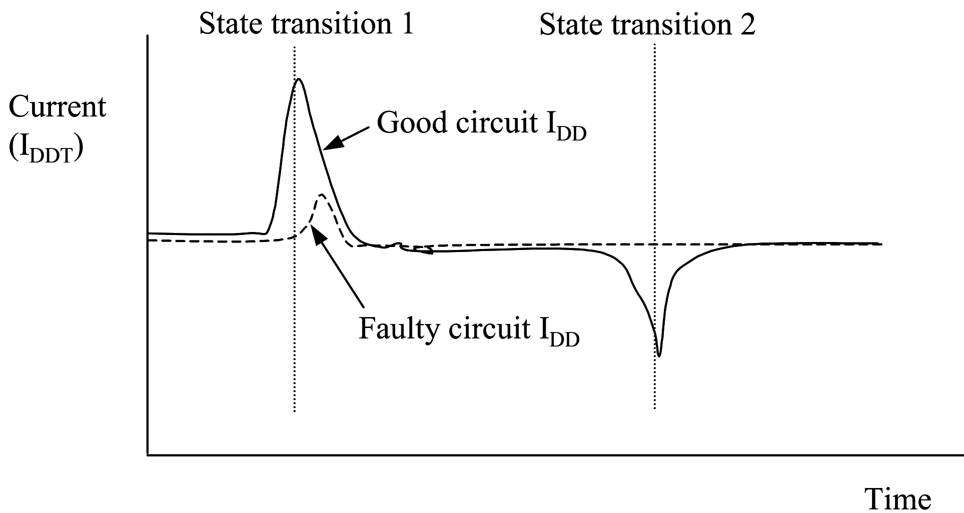

Fig. 2. Comparison of good circuit I_{DDT} response to faulty circuit I_{DDT} response.

3. PRINCIPLE OF I_{DDT} TEST

I_{DDT} test measures transient current instead of static leakage [20][21]. The I_{DD} waveform shows a spike whenever the circuit makes a transition from one logic state to another logic state (see Figure 2). The dynamic current depends on the switching activity during the transition (which and how many transistors switch, the path taken by the current, etc.). The presence of a defect alters the nature of the current transition that can be used to differentiate fault-free and faulty circuits. The feasibility of I_{DDT} testing has been proposed earlier [22][23][24] and it is shown to be capable of detecting certain stuck-open defects that cannot be detected by I_{DDQ} and other test methods [25]. The differentiation between faulty and fault-free I_{DDT} waveforms can be achieved by measuring the number of transitions between the two logic states, or by comparing I_{DDT} waveform with a "golden" (fault-free) signature [26].

Although I_{DDT} test does offer certain advantages over I_{DDQ} test, the measurement of transient current is more difficult than static leakage and the instrumentation setup required for this purpose is expensive. The decoupling capacitance may smoothen out I_{DDT} waveform making defect-free and defective waveforms indistinguishable. Moreover, since "I_{DDT}-fail" does not necessarily mean defective, the threshold setting issue similar to I_{DDQ} test exists for I_{DDT} test as well [27].

4. ADVANTAGES OF I_{DDX} TESTS

I_{DDX} testing offers several advantages [28]. Defect detection requires that the defect be excited (activated) and its effect be propagated to an output. Thus, any test needs to satisfy both excitation and propagation conditions. This is difficult for voltage-based structural tests like stuck-at test [29]. Since I_{DDX} uses power supply lines for observation, there are no special propagation requirements. Since it offers 100% *observability* test generation effort involves only excitation of possible defect sites [30]. Only a few vectors are usually enough to achieve reasonably high fault coverage [31]. I_{DDQ} test is shown to be useful for fast fault localization [32][33] by using multiple fault models. Gate level fault models assume that defects occur on the nets (on the periphery of a gate). Therefore, certain real defects may not have a gate-level fault model, but can still be detected by I_{DDX} test. This can result in higher than estimated fault coverage using the pseudo stuck-at fault model [34]. I_{DDX} tests are superior than voltage-based tests in detecting shorts [35].

I_{DDQ} test is capable of detecting *weak* ICs or ICs with latent defects that pose a reliability risk [36][37]. This includes metal slivers, electromigration-induced defects, hot carrier injection damage, etc. [38]. Thus I_{DDQ} test can be employed to screen such devices for high-reliability applications. The traditional method of ensuring high reliability is burn-in (BI) test, in which chips are subjected to temperature and voltage stress to accelerate latent defects [39]. However, as supply voltage is scaled down and operating temperature is increased, the effective voltage or temperature stress is reduced. This reduces the effectiveness of BI for DSM technologies. Moreover, BI is getting prohibitively expensive. The potential of I_{DDX} test to eliminate [40][41][42] or reduce BI has been investigated [43][44]. Another alternative for screening weak chips are VLV testing [45] and MinVDD test [46].

It has been observed that certain defects can be detected by I_{DDX} test only. Therefore, many semiconductor manufacturers have used I_{DDX} test to improve the quality of the existing test suite consisting of functional and scan test vectors [47][48]. The improvement of 5-10% in the production line fallout rate (percentage of total chips rejected after system level testing) after adding I_{DDX} test has been reported [49]. This improvement was achieved after high stuck-at fault coverage (>99%) was used. However, it must be emphasized that an I_{DDX} test complements functional and other structural tests [50], and cannot replace them [51].

5. CHALLENGES FOR I_{DDQ} TEST

Traditional I_{DDQ} testing has followed a simple approach called the single or *static threshold method*. Several I_{DDQ} measurements are taken for a chip and if any measurement exceeds the threshold, the chip is considered to be defective. The threshold is determined either by circuit simulation or empirically. While this approach has worked for earlier technologies, for reasons explained later, it is not suitable for new and emerging technologies.

As transistor geometries are reduced, it is necessary to reduce the supply voltage to avoid electrical breakdown and to reduce power consumption. However, to retain or improve performance it is necessary to reduce the transistor threshold voltage (V_{TH}) as well. The sub-threshold leakage current of a MOSFET is given by

$$I_{sub} = \mu\, C_{ox} \frac{W}{L} V_t^2 e^{V_{GS} - V_{TH} / \eta V_t} \cdot (1 - e^{-V_{DS} / V_t})$$

where μ is the carrier mobility, C_{OX} is the gate capacitance per unit area, W is the channel width, L is the channel length, V_{GS} is the gate-to-source voltage, V_t is the thermal voltage, V_{TH} is the threshold voltage and η is a technology dependent parameter [52][53]. Thus, the reduction in threshold voltage (V_{TH}) causes an exponential increase in the sub-threshold leakage current [54][55]. Due to increasing number of transistors, mixed-signal designs, and reduced threshold voltages, leakage current levels are rising with each technology node [56]. The International Technology Roadmap for Semiconductors (ITRS) projections for fault-free leakage currents at room temperature (25°C) for future generation high-performance ICs shown in Table I suggest that distinguishing defect current in the presence of large background current will become extremely difficult.

Moreover, controlling transistor geometries precisely becomes harder for smaller transistors. This results in large variation in fault-free I_{DDQ}. As fault-free and faulty I_{DDQ} distributions overlap, it is not possible to discriminate faulty chips. This reduces the defect screening resolution of I_{DDQ} testing and raises concerns about the applicability of I_{DDQ} test in the future [57][58][59][60][61]. As conceptually illustrated in Figure 3, any single I_{DDQ} threshold invariably results in false rejects (yield loss[1]) and/or false accepts (test escapes). Understanding whether the I_{DDQ}-only failed chips are defective or fault-free is important to

[1] The term yield loss is somewhat misleading for high-performance chips. Since I_{DDQ} failures are unique in nature, in the absence of the I_{DDQ} test, some of these chips may have resulted in customer returns. Handling a customer return costs more than the chip itself and damages the manufacturer's reputation.

minimize yield loss [62]. The I_{DDQ} levels and variations are expected to grow as transistor geometries are scaled further [63]. Hence I_{DDQ} test is considered a difficult challenge by the ITRS. The advent of DSM technologies is therefore considered the end of single threshold I_{DDQ} testing [64][65].

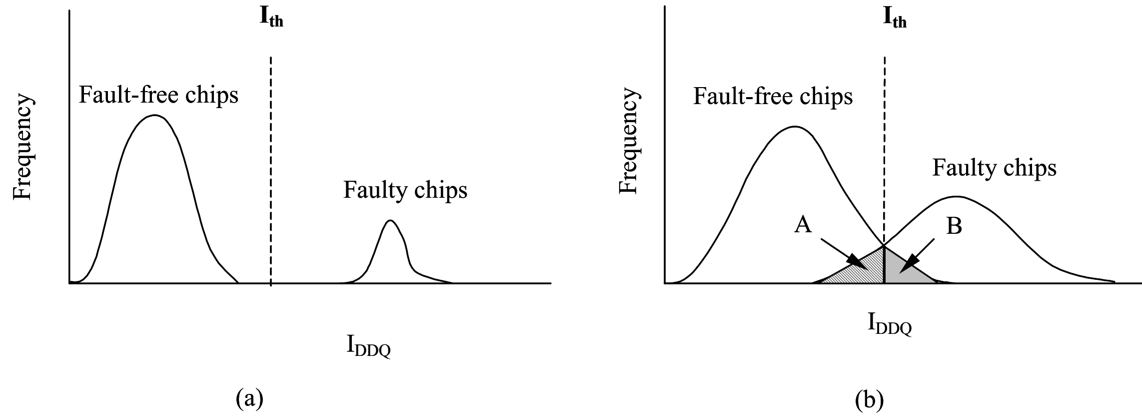

Fig. 3. (a) Single threshold test that could distinguish between faulty and fault-free distributions for earlier technologies (b) causes yield loss (region B) and/or test escapes (region A) for DSM technologies.

6. REVIEW OF I_{DDQ}-BASED TESTS

To retain the effectiveness of I_{DDQ} test in production without causing excessive yield loss, several solutions have been proposed in the literature. The problem with I_{DDQ} test is straightforward: faulty and fault-free currents are indistinguishable due to increased magnitude and variance in the fault-free I_{DDQ}. Researchers have approached this issue in three different ways:

1. Use an additional parameter that correlates with I_{DDQ} to estimate I_{DDQ} for each chip.
2. Estimate fault-free I_{DDQ} for each chip using elaborate device models.
3. Use data analysis methods for variance reduction to distinguish between faulty and fault-free I_{DDQ}.

These methods are summarized in Table II and reviewed in the following sections.

6. 1 Use of Secondary Parameter for I_{DDQ} Testing

Use of another parameter adds another dimension to the existing I_{DDQ} data and provides an effective way to screen defective chips.

6.1.1 I_{DDQ} versus Temperature

The fault-free I_{DDQ} has an exponential relationship with temperature [66]. Faulty or defective current does not show such a relationship. The dependence of fault-free leakage on temperature can be exploited by making current measurements at two temperatures. The defective current may remain the same or decrease (due to a positive temperature coefficient for a resistive metal short) with an increase in temperature. This makes differentiation between fault-free and faulty chips possible [67]. Testing can be performed by measuring I_{DDQ} at room temperature and either at a reduced [68] or higher [69] temperature. Low temperature measurement is undesirable in production due to high cost. It is possible to make additional I_{DDQ} measurements at elevated temperatures by using hot wafer chuck.

6.1.2 I_{DDQ} versus F_{max}

I_{DDQ} and transistor delay both depend on transistor effective channel length (L_{eff}). The smaller the channel length, the faster the transistor and the higher is the leakage. The maximum frequency (F_{max}) a chip is capable of operating at is therefore related to the intrinsic leakage current. Some researchers have used the correlation between these two factors to screen defective chips [70]. The F_{max} can be estimated by using test structures embedded in the chip, like ring oscillators. The advantage of exploiting this correlation is that fast and leaky chips can be distinguished from defective chips at the wafer level. The pass/fail thresholds could be adjusted to reduce yield loss. For chips using Level Sensitive Scan Designs (LSSD) [71] flush delay is shown to correlate with leakage current [72] (Figure 4). IBM has used correlation between I_{DDQ} and ring oscillator delay for screening defective chips in production [73].

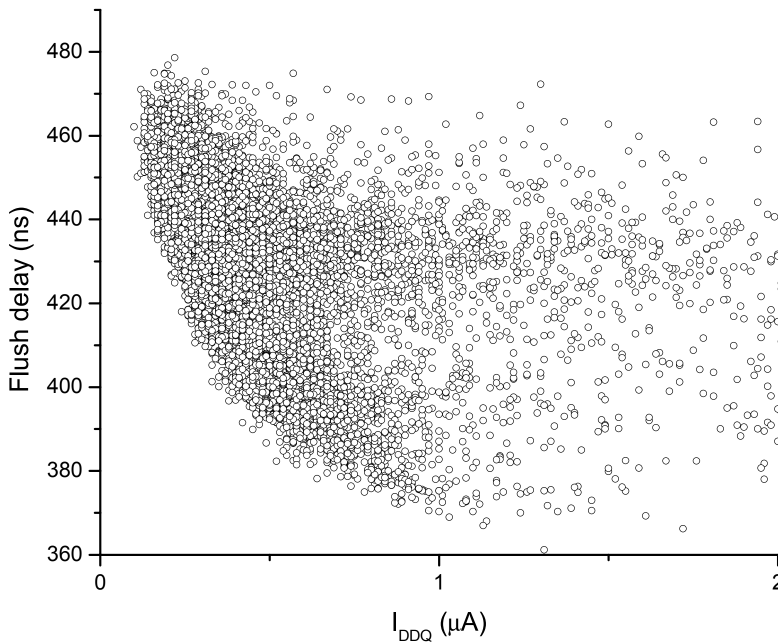

Fig. 4. Flush delay and I_{DDQ} show strong correlation especially for small I_{DDQ} values.

6.1.3 Light-based I_{DDQ} Test

The device characteristics are affected by electron-hole pairs generated by photons. This fact is used in light-based I_{DDQ} test [74]. In this method, two I_{DDQ} measurements, one with light and the other without light, are taken. When exposed to light, leakage current increases due to photoconductivity. This increase is uniform for all chips whether they are faulty or fault-free. Some transistors with floating gates switch when exposed to light. This changes the background leakage current. The difference in the dark current (I_{DDQ} when the device is not exposed to light) and the lighted current (I_{DDQ} when the device is exposed to light) is used to screen defective chips. This method is applicable only at the wafer level, is affected by ambient light conditions, and is very sensitive to light intensity. Moreover, the resolution depends on several factors such as photoconductivity of materials, light intensity, and number of switching transistors.

6.2 Model-based I_{DDQ} Estimation

As yield loss caused by I_{DDQ} test became a matter of concern, research efforts were directed towards accurate estimation of the leakage current for accurate threshold setting. Although research for estimating defective I_{DDQ} has been reported [75], due to infinite possibilities of defects it is easier to estimate maximum permissible fault-free I_{DDQ} [76]. In the I_{DDQ} estimation method, the models are built for each cell or gate in the cell library [77]. The chip I_{DDQ} is estimated by parsing the entire netlist and determining maximum I_{DDQ} for each input vector [78]. For DSM chips it is necessary to have a model that can account for process variations. The correlation between different vectors can be exploited to achieve this [79][80]. However, selecting I_{DDQ} threshold even through characterization [81] is difficult due to manufacturing variations [82][83].

6.3 I_{DDQ} Variance Reduction/Data Analysis Techniques

The overall goal of variance-reduction techniques is post-process parametric test data for screening defective chips. The main advantage of these methods is very little investment. In some cases, Automatic Test Equipment (ATE) needs to be modified or a new load board may be needed. In other cases the ATE software may need to be reconfigured. Compared to design or process changes these modifications take much less time and investment, and are relatively easy to implement. The downside is that the effectiveness of these methods depends on process stability.

6.3.1 Current Signature

Proposed by Gattiker and Maly [84][85], this method relies on the graphical display of I_{DDQ} readings sorted in ascending order. It relies on the premise that I_{DDQ} for an active defect is higher (for vectors that excite it) than normal leakage. Thus, the presence of a “step” or “jump” in a signature indicates the presence of at least two distinct leakage paths or an active defect. In the case of a passive defect, this assumption is violated as defect excitation is independent of the input pattern. Thus the current signature of a chip with a passive defect does not show any “steps” and can be indistinguishable from the fault-free current signature. If the background leakage is small, to a certain extent the step size is indicative of severity of the defect. Figure 5 shows the current signatures for three chips. Chip ‘A’ is fault-free and has a smooth signature. The small steps are due to intra-die variance in I_{DDQ} and slightly different leakage paths for each vector. Chip ‘B’ has an active defect as indicated by steps in the signature. Chip ‘C’ shows a smooth signature similar to that of chip ‘A’, but all I_{DDQ} values are higher by an order of magnitude. This chip is therefore likely to contain a passive defect.

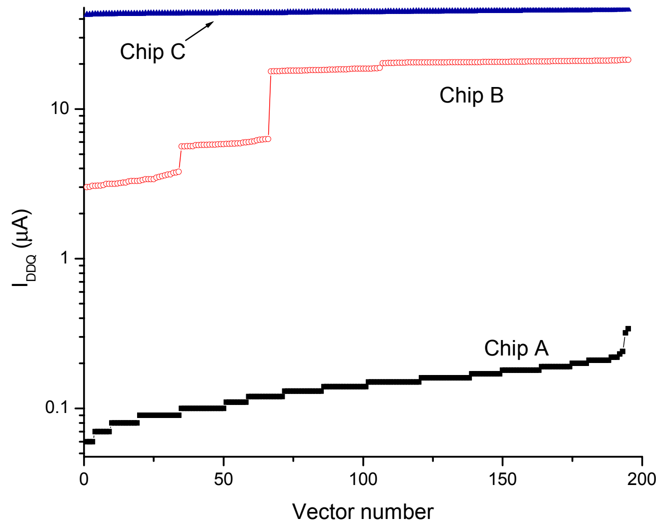

Fig. 5. Current signatures for a fault-free chip (Chip A) is smooth and that for a chip with an active defect (Chip B) shows steps. Chip C has a passive defect and has a smooth signature.

To be effective, current signature requires several I_{DDQ} measurements. Since quiescent leakage can be measured only after internal circuit activity is settled down, I_{DDQ} is a slow test and measuring I_{DDQ} for many vectors can be achieved by designing special purpose measurement circuitry like QuiC-Mon [86]. An alternative production implementation of the signature-based approach [87] suggests making an initial measurement and placing a guard band around it. If any later measurement falls outside this guard band, the chip is rejected.

In spite of its simplicity, current signature is very effective. Current signatures are useful for performing fault diagnosis as well [88][89]. A lot of information about the circuit (*circuit personality*) can be gleaned from the analysis of current signatures [90]. Two practical issues, however, must be dealt with. The first is deciding how many measurements are enough. The second is deciding the maximum fault-free step size. Both these issues directly impact test time (and hence, test cost), yield loss (false rejects) and test escapes (quality). Such wafer-level post-processing of data is becoming increasingly important for new technologies as process variations increase [91].

6.3.2 Delta I_{DDQ}

In the delta I_{DDQ} method [92][93][94][95] differences (deltas) between I_{DDQ} values for successive test vectors (*successive pattern method*) for a chip are obtained. Thus delta I_{DDQ} is defined as:

$$\Delta I_{DDQ}(i) = I_{DDQ}(i) - I_{DDQ}(i\text{-}1)$$

where $I_{DDQ}(i)$ and $I_{DDQ}(i\text{-}1)$ are I_{DDQ} readings for the ith and $(i\text{-}1)^{th}$ vectors. For a fault-free chip, only intrinsic variation in I_{DDQ} causes the mean delta I_{DDQ} to be close to or equal to zero and the variation in deltas to be small. The screening can be performed if any absolute ΔI_{DDQ} surpasses the maximum permissible threshold or if the variance in the ΔI_{DDQ} values is too large (*consecutive vector method*). Another alternative is to determine the difference between maximum I_{DDQ} and minimum I_{DDQ} and reject the

chip if the difference exceeds the ΔI_{DDQ} limit (*max-min method*). This method assumes that at least one vector excites the defect and the defective I_{DDQ} is much higher than the fault-free I_{DDQ}.

Delta I_{DDQ} is shown to be superior to the conventional single threshold approach [96] and an order of magnitude resolution enhancement using an FFT technique has been reported [97]. In the case of a passive defect, since all readings are elevated, deltas are small. Hence this method is unable to screen chips with a passive defect. The robustness of delta I_{DDQ} can be improved by sorting individual readings and then obtaining deltas. This method, called 2nd order analysis, combines the features of current signature and delta-I_{DDQ} [98].

Figure 6 illustrates the histograms of delta I_{DDQ} for three chips. All chips passed all Boolean tests. In each case, a total of 194 deltas are obtained by subtracting readings for two consecutive vectors. Figure 6(a) is a histogram for a fault-free chip that exhibits small mean value and variation. Figure 6(b) is the histogram for a chip with an active defect. Such a chip typically exhibits large variation in delta I_{DDQ}. Figure 6(c) underscores the difficulty in screening a chip with a passive defect as the variation in deltas is small.

The production implementation of delta-I_{DDQ} may consist of making a measurement and setting a guard band around this value [87]. If any later reading falls outside this guard band, the chip is considered defective and is rejected. The width of the guard band needs to be determined through characterization of fault-free chips. A speed-dependent approach for delta-I_{DDQ} that considers additional test circuit speed data has been reported [99].

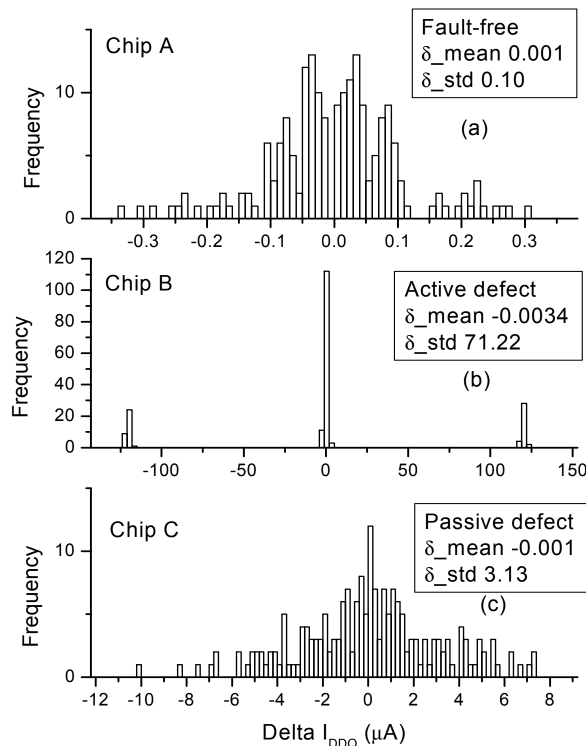

Fig. 6. Smaller variance in delta-IDDQ distribution distinguishes a fault-free chip (Chip A) from a faulty chip (Chip B), but not a chip with a passive defect (Chip C).

Although delta I_{DDQ} is intuitively simple and easy to implement, it also suffers from the same issues as current signature. The number of measurements limit the defect screening resolution of delta-I_{DDQ}. Deciding the maximum fault-free delta is not trivial as it requires elaborate vector sensitivity analysis (which paths are turned ON/OFF) as well as process sensitivity analysis (impact of process variations on intrinsic I_{DDQ}). The state-dependent leakage differs from die to die due to process variations across a wafer. Moreover, stochastical process variations lead to within-die variations in the leakage current apart from the pattern dependent variation. This variation becomes important as background leakage becomes more than 10 mA thus making the future of delta-I_{DDQ} questionable for DSM technologies [100].

6.3.3 Statistical Clustering

Clustering is a statistical procedure of sorting data into groups such that the degree of "natural association" is high among members of the same group and low between members of different groups. It uses correlation or other such measure of association for classifying the data into groups. In a loose sense, it can be considered as multi-dimensional regression. Some experiments of the application of clustering techniques to I_{DDQ} testing have been reported [101][102]. Figure 7 shows a typical result of clustering. The chips are divided into four clusters. Notice that chips having similar I_{DDQ} can be clustered into different groups. Thus, seemingly fault-free chips can be grouped with defective chips and vice versa.

In principle, clustering can be applied to any continuous parameter. For example, clustering I_{DDQ} data combined with chip speed can be helpful in finding outliers with higher confidence. Due to its nature of grouping elements, clustering inherently accounts for process variations. However, it requires a number of readings to be meaningful. Ideally, data should get grouped into two clusters: one defective and the other not. But in practice, data get divided among many clusters and it is up to the user to decide which groups represent faulty and fault-free chips. This is not trivial because as the number of clusters increases, they tend to overlap due to the underlying correlation between different vectors. On the other hand, if the number of clusters is reduced (by an input parameter to the statistical analysis software), the distinction between fault-free and faulty chips fades.

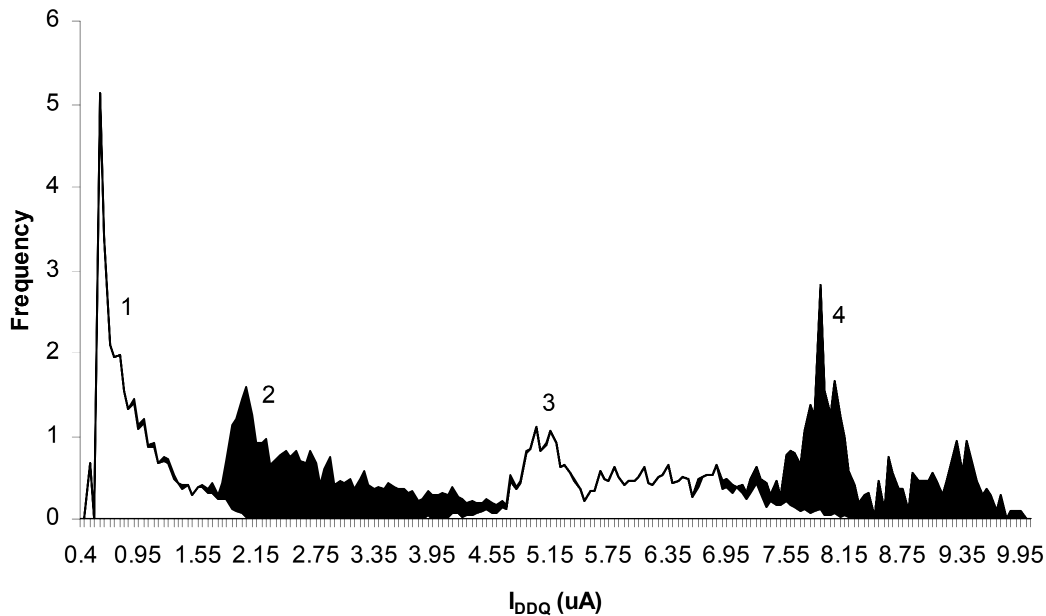

Fig. 7. Normalized histograms for four clusters.

6.3.4 Current Ratio

In spite of the increased magnitude and variation in I_{DDQ} in new technologies it was observed that the ratio of maximum I_{DDQ} to minimum I_{DDQ} (called *current ratio*) for fault-free chips is relatively the same [103]. A leaky chip will leak proportionately more for *all* vectors and, therefore, its current ratio will be comparable to fault-free current ratios. Through characterization the input vectors that cause minimum and maximum I_{DDQ} are determined and current ratio is obtained. To account for process variation a guard band is added. Figure 8 shows current ratios sorted in ascending order for several all-pass (passed all Boolean tests with $I_{DDQ} < 5$ μA) and I_{DDQ}-only failed (passed all Boolean tests with $I_{DDQ} > 5$ μA) chips from SEMATECH test data. Clearly, the I_{DDQ}-only failed chips exhibit more spread in current ratios than the fault-free chips. However, even for all-pass chips current ratios show variation of more than an order of magnitude. Several defective chips have current ratios (less than 10) comparable to all-pass chip current ratios. Therefore, deciding the appropriate current ratio can be challenging. For passive defects, the current ratio reduces with increasing background leakage. Determining a lower threshold for current ratios, however, is difficult due to the fast falling distribution near the current ratio values of one [104].

6.3.5 Eigen Signatures

Methods like delta I_{DDQ}, current signature and current ratio essentially exploit the regularity in I_{DDQ}. Defects induce distortion in the observed regularity and can be detected. Okuda proposed a method that exploits this regularity by taking the ratio of I_{DDQ} for each vector to the mean I_{DDQ} [105]. He suggested five different signatures called *Eigen signatures* that exploit this regularity for detecting defects [106]. An example of eigen signature is normalized Z-score obtained as follows:

$$E_{NIQ(i)} = \frac{I_{DDQ(i)} - \overline{I_{DDQ}}}{\sigma I_{DDQ}}$$

where $E_{NIQ(i)}$ is the normalized I_{DDQ} value (Z-score), $I_{DDQ}(i)$ is I_{DDQ} for i^{th} vector, $\overline{I_{DDQ}}$ is the mean I_{DDQ} value and σ_{IDDQ} is standard deviation across all vectors. Figure 9 shows the variation in the mean and intra-die standard deviation for SEMATECH chips that passed all voltage-based tests. Although regularity is visible, there is large deviation in both values.

The success of the eigen signature-based approach depends on the underlying process as that governs the regularity in the signature. It is also necessary to have a large number of measurements for successful implementation.

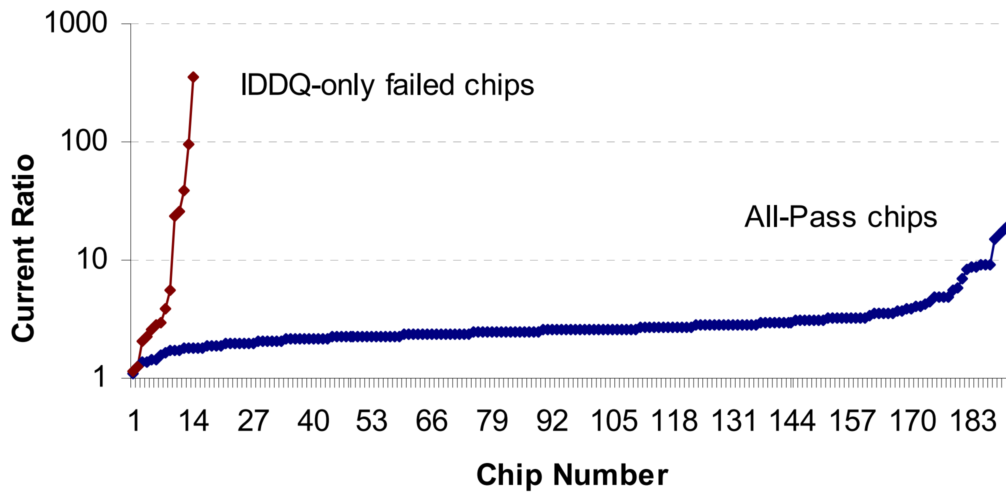

Fig. 8. Current ratios of fault-free chips from a wafer show small variation to those of faulty chips.

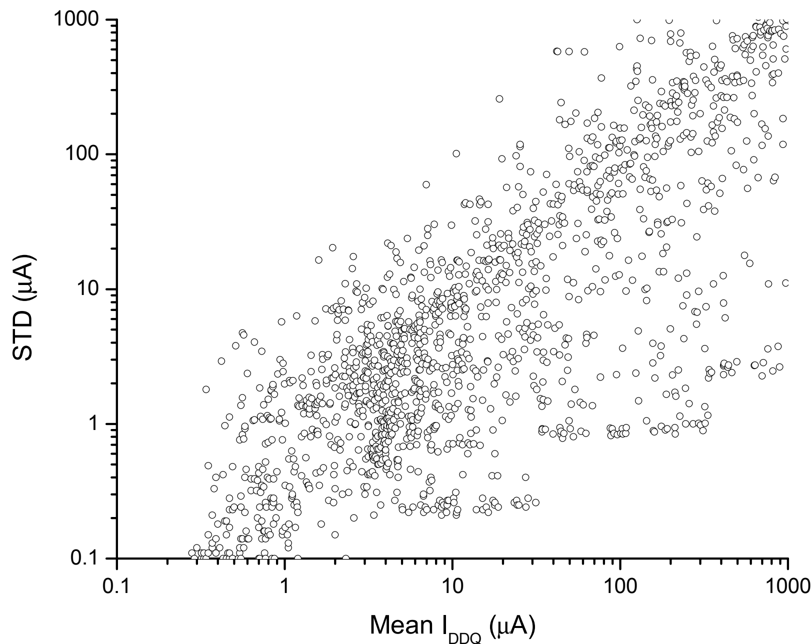

Fig. 9. Scatter plot of mean and intra-die standard deviation of SEMATECH chips shows regularity in I_{DDQ}.

6.3.6 Statistical Outlier Rejection Methods

Figure 10 shows the distribution of I_{DDQ} values for a vector across many different chips. All these chips passed Boolean tests. Notice that the distribution has a long tail. Obviously the chips in the tail have a different leakage mechanism than those in the central part of the distribution. However, determining whether that is process-induced or defect-induced is extremely difficult. From a statistical perspective the chips exhibiting abnormal behavior are *outliers*. Hence it is possible to use outlier rejection methods to screen defective chips [107][108]. The basic idea behind outlier rejection is that if the variance in the parameter for a chip cannot be explained by fault-free mechanisms, the chip must be defective. For high-reliability requirements it is suggested that *being different* is reason enough for suspecting and/or rejecting chips even if they pass all functional or structural tests [109]. This becomes important as tests lose their resolution in DSM era [110].

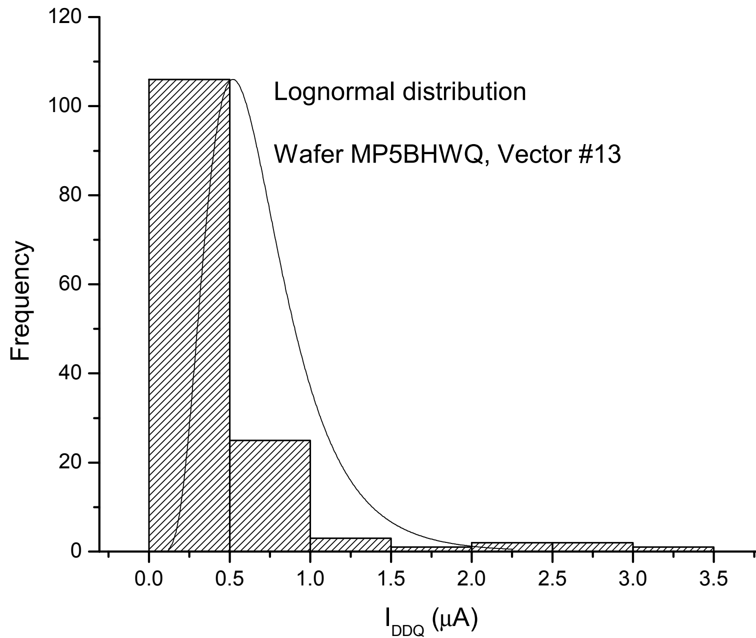

Fig. 10. I_{DDQ} distribution of chips from a wafer show a long tail and chips with leaky chips as outliers.

Outlier rejection methods however may make assumptions about the distribution (e. g. Normal). If the distribution does not satisfy these requirements, appropriate transforms must be used. In some cases, determining such transformation may be difficult or infeasible [104].

6.3.7 Wafer-level Spatial Correlation Methods

Since the neighboring chips on a wafer undergo similar process changes, their fault-free parameters are correlated. Also, due to defect clustering a chip with more defective neighbors is more likely to fail than others. This concept was explored for test cost reduction and defect level prediction earlier [111][112]. It can be exploited to estimate maximum fault-free leakage and screen defective chips [113]. Figure 11 shows that neighboring fault-free chips on a wafer have similar I_{DDQ}. Some chips have higher leakage current than their neighboring chips. These chips are called *spatial outliers*. The basic philosophy of all spatial correlation methods is to decompose wafer-level spatial data and identify high-frequency spatial variation [114]. Since no fault-free mechanism can explain sudden change in parameters of neighboring chips it is considered indicative of a defect. Several methods that use wafer-level spatial correlation for screening defective chips have been proposed [115]-[121].

A. Spatial fit method

In Figure 11, notice that except for a few spatial outliers, neighboring die have similar I_{DDQ} readings. This method exploits this fact to estimate maximum fault-free I_{DDQ} of a die using I_{DDQ} data and die XY-position information of adjacent die through linear regression [115]. Considering I_{DDQ} as the third dimension (Z-value), the estimate of fault-free values is the best fit plane value. The actual value is subtracted from the estimate to obtain residuals. If residuals exceed a pre-determined threshold, the die is

considered defective. When adjacent die I_{DDQ} data are not available (e. g. die on the wafer edge or functional fails in a stop-on-first-fail test flow) die at longer distances may be used.

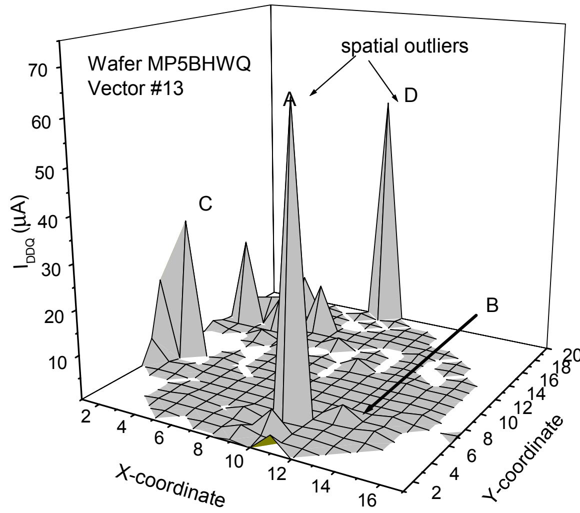

Fig. 11. Neighboring fault-free chips on a wafer have similar I_{DDQ}. Some spatial outliers are visible.

B. Nearest Neighbor Residual (NNR)

This method is similar to the spatial fit method. However, the median or mean I_{DDQ} of neighboring die is used as an estimator of I_{DDQ} of the center die [116]. High residual values are considered indicative of defective chips. The study of correlating neighbors was shown to be useful for robust outlier screening [117]. In a recent study, the applicability of wafer-level post-processing to other parametric test data was validated and the improvement in the early failure rate (EFR) was shown [118].

Although NNR is a valuable variance reduction technique, its effectiveness depends on the smoothness of the wafer pattern. In case of stepper field patterns, it is necessary to identify neighbors that exhibit high correlation [117].

C. Neighbor Current Ratio (NCR)

This method exploits the fact that two neighboring fault-free die on a wafer have similar I_{DDQ} values for the same vectors. Therefore, the ratio of I_{DDQ} of a die and that of its neighbor for the same vector should be close to 1 if both die are fault-free. This ratio is termed the Neighbor Current Ratio (NCR) [119]. The NCR is self-calibrating since ideally (for fault-free chips under no process variations) NCR is equal to 1 [120]. Of course, owing to process variations NCR values vary. NCRs are obtained for all vectors considering all adjacent neighbors. The maximum value of NCR is used for screening defective chips.

Mathematically, NCR is defined as follows:

$$NCR_{ji} = \{\frac{I_{ci}}{I_{ji}}\} \quad \forall i \, and \, 1 \le j \le 8$$

where I_{ci} is I_{DDQ} of the center die for the ith vector and I_{ji} is I_{DDQ} of the jth neighboring die for the ith vector. Figure 12 shows NCR variation across the wafer shown in Figure 11. Notice that several chips have high NCR values (spatial outliers) and are likely to be defective.

A combination of CR and NCR shown in Figure 13 can improve defect screening [104]. Using CR and NCR thresholds, plot can be divided in four quadrants as shown. The chips in the upper left quadrant are mostly passive or subtle active defects that cannot be detected by CR alone while those in the upper right quadrant are gross outliers that can be screened by either method. The chips in the lower right quadrant are outliers surrounded by defective chips (outliers in a bad neighborhood) that cannot be detected by NCR alone. Good (fault-free) chips or chips with subtle defects in a bad neighborhood get grouped in lower left quadrant. This technique remains applicable for state-of-the-art technologies as shown in Figure 14 for 180 nm technology data from LSI Logic.

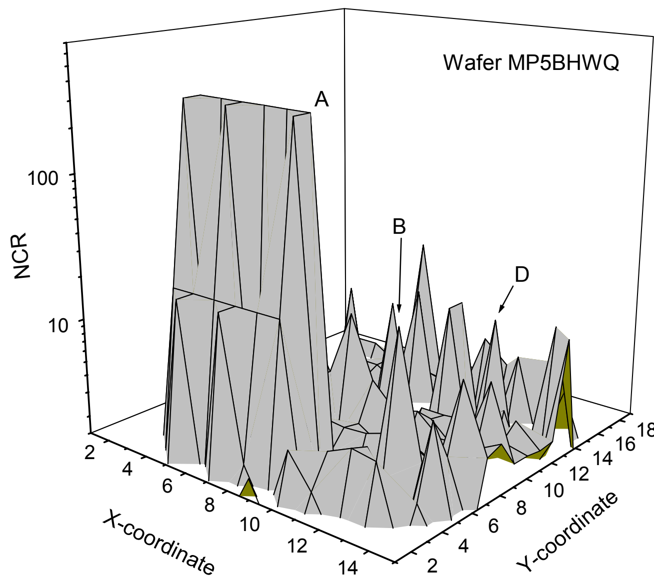

Fig. 12. NCR Variation across a wafer.

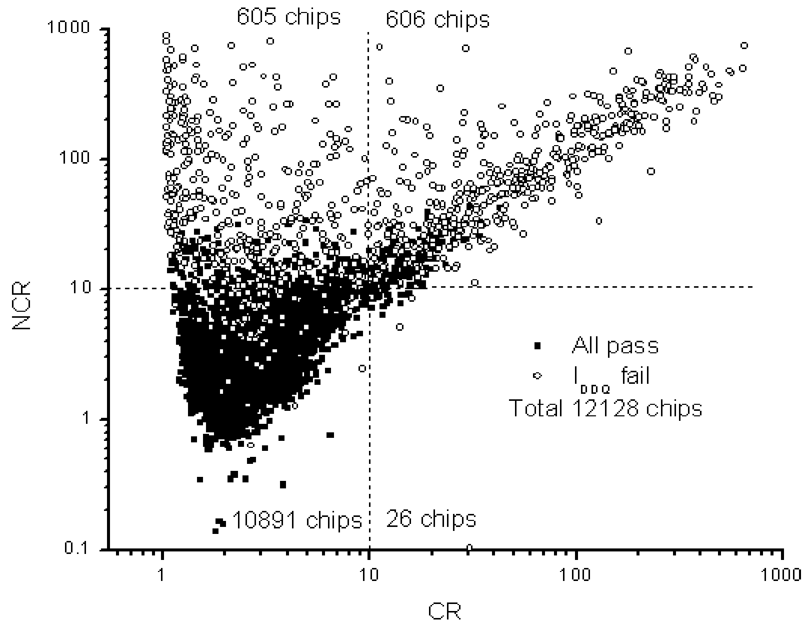

Fig. 13. CR-NCR scatter plot for SEMATECH chips that passed all Boolean tests and have I_{DDQ} < 100 µA. The number of chips in each quadrant is shown.

D. Immediate Neighbor Difference I_{DDQ} Test (INDIT)

This method is similar to NCR, but instead of ratios of two I_{DDQ} values, differences in two I_{DDQ} readings are obtained [121]. Since fault-free I_{DDQ} values are similar, the difference is expected to be close to zero. In a sense, this is a variation of delta-I_{DDQ} [93] method where wafer-level information is added to the I_{DDQ} data. The conventional delta I_{DDQ} uses maximum intra-die delta (*self-delta*) whereas INDIT uses maximum inter-die delta (*neighbor-delta*) for screening defective chips. Figure 15 shows variation of maximum self-deltas across a wafer. The variation of maximum neighbor-deltas shown in Figure 16 illustrates that several die on this wafer are likely to contain passive defects (or a combination of active and passive defects) that are not screened by self-delta alone.

The neighboring chip variance in fault-free parameters does not change appreciably with advances in technology. Therefore, all wafer-level spatial correlation methods will remain applicable to later technology nodes. However, they will become less effective as intra-die variance increases. Another limitation of the spatial methods is that they can be misleading due to defect clustering [122].

6.3.8 Principal Component Analysis-based Linear Prediction

Recently the use of a Principal Component Analysis (PCA)-like method to estimate fault-free I_{DDQ} has been reported [123]. This method exploits the fact that device leakage currents of fault-free devices are correlated to each other through the underlying set of process parameters. It uses a sample of data to train a model and then uses this model for analyzing other chips. Thus the I_{DDQ} value of one test vector can be predicted from the I_{DDQ} values of one or more other test vectors. If the prediction is accurate, residuals are small for fault-free chips and faulty chips can be identified. The estimation accuracy (and hence the outlier screening resolution) depends on the data set used to train the model. Outliers in the training data set can bias the estimation, thus resulting in test escapes.

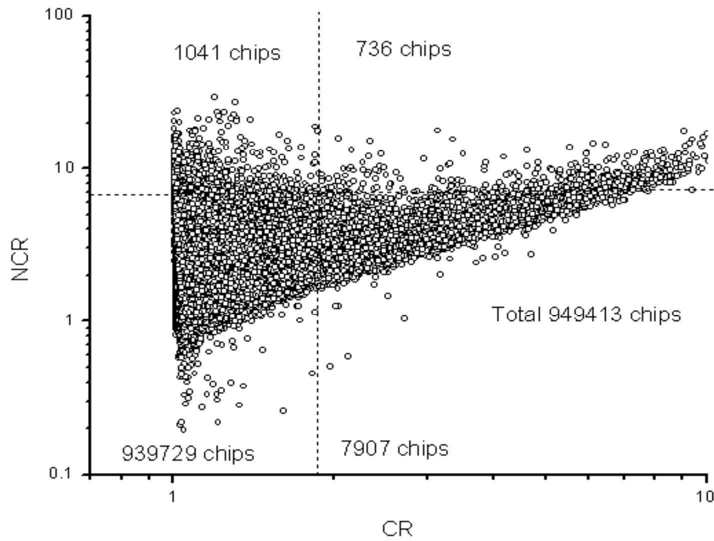

Fig. 14. CR-NCR scatter plot for LSI Logic data.

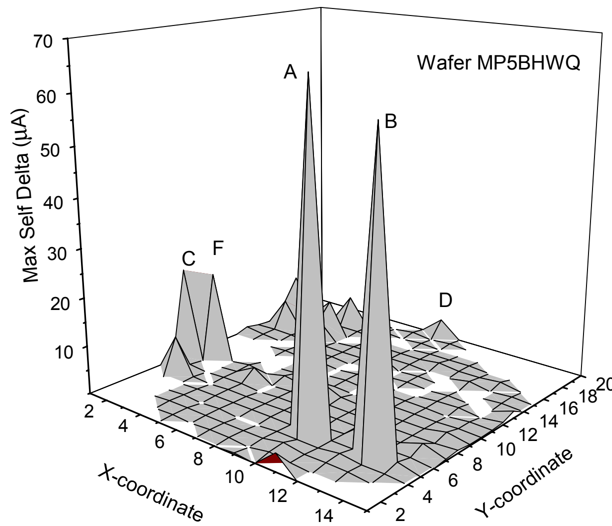

Fig. 15. Wafer surface plot of maximum self-delta (within chip delta).

7. REVIEW OF I_{DDT}-BASED TESTS

In a sense, I_{DDT} test is the counterpart of I_{DDQ} test. It offers all the advantages of I_{DDQ} test such as no propagation requirement, high fault coverage to vector ratio, etc. Moreover, since the measurement circuit does not require internal circuit activity to settle down, I_{DDT} tests are faster than I_{DDQ} tests. However, all I_{DDT} methods necessarily require high-speed measurement circuitry with high accuracy. They also require multiple samples for waveform analysis. Unlike I_{DDQ} tests, I_{DDT} tests are not restricted to static CMOS circuits and have high resolution for large ICs. They are capable of detecting certain delay faults and open defects as well [124]. I_{DDT}-based tests in conjunction with FFT have been shown to be useful for fault diagnosis [125]. Of course, similar to other I_{DDQ} test methods, defining the fault-free (golden) I_{DDT} signature is difficult. The load board and on-chip decoupling capacitors filter high-frequency spikes and blur the distinction between fault-free and faulty chips. These methods are summarized in Table III.

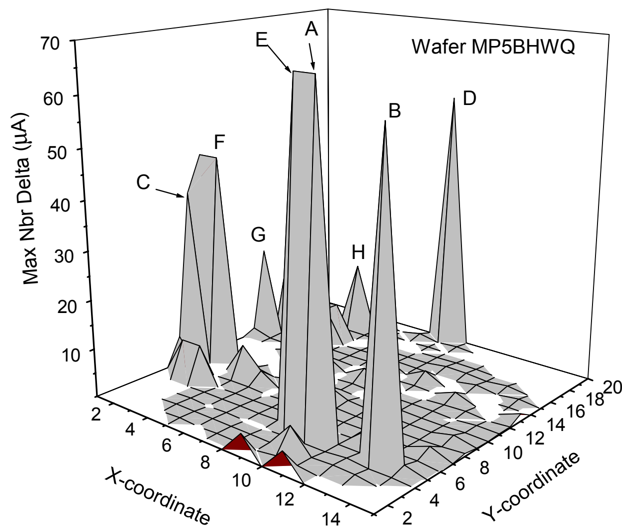

Fig. 16. Wafer surface plot of maximum neighbor deltas. Some outliers not detected by delta-IDDQ now become visible.

7.1 I_{DD} Pulse Response Testing (PRT)

In PRT [126][127], both power supply rails are pulsed simultaneously from the midpoint voltage to their nominal values (e. g. V_{DD} rail from $V_{DD}/2$ to V_{DD} and V_{SS} rail from $V_{DD}/2$ to 0) while bias voltages to all inputs are set to the midpoint value. During pulsing, transistors enter either sub-threshold, linear or saturation region and their current characteristics can be observed. This method is vector independent, suitable for both digital and analog circuits and capable of detecting gate oxide shorts, opens, and poly or metal bridges [126]. The authors showed that analysis can be done in time or frequency domain. As supply voltages are scaled down, the effectiveness of PRT diminishes as the absolute voltage difference between two logic states becomes smaller. Pulsing both rails also results in loss of logic state and with increased number of transistors per chip, the distinction between faulty and fault-free chips fades.

7.2 Dynamic Power Consumption Current-based Testing

Figure 2 shows a typical I_{DDT} response for a good and a faulty circuit. Note that the defect is not detectable by I_{DDQ} measurement alone since there is no appreciable change in the quiescent value of the current. The power consumption peaks occur because for a brief period of time both PMOS and NMOS transistors conduct simultaneously, thus short circuiting the power supply. The current decays exponentially due to capacitive charge/discharge in the circuit. In this method, an integrator circuit is used to measure the dynamic power consumption of the circuit. Since the integral of current is the total charge delivered to the circuit, this method is also called Charge Based Testing (CBT). The charge is recorded by applying state transition test vectors (STTVs) at the input of a chip. The output voltage of the integrator is proportional to the dynamic power consumption of the circuit. If this value deviates the predetermined threshold, the chip is considered defective. Results of application of dynamic power consumption current testing show that I_{DDT} testing is capable of detecting certain open and parametric defects not detectable by I_{DDQ} test as they do not result in increased leakage [128][129]. It is shown to be useful for detecting defects

in static RAMs [130][131]. It is necessary to obtain a good set of STTVs since those ultimately decide the sensitivity of this method. Similar techniques are shown to be capable of detecting bridging defects in static CMOS [132] as well as domino CMOS circuits [133].

7.3 Transient Signal Analysis (TSA)

TSA is based on a measurement of the contribution to the transient response of a circuit by physical characteristics such as substrate, power supply, and parasitic capacitive coupling [21]. In this method, transients are analyzed at multiple test points [134]. Under the assumption that process variation is uniform across a die, TSA can distinguish between the changes in the transient response caused by defects and those caused by process variation. If changes are caused by process variation, the transients are correlated for fault-free devices. On the contrary, the presence of a defect alters transients at test points closer to the location of the defect. Recent studies indicate that TSA is helpful for defect localization [135][136] and detecting delay defects [137].

7.4 Frequency Spectrum Analysis of Dynamic Current

Analysis of frequency spectrum of transient waveform for fault detection has been investigated. Thibeault proposed sampling the I_{DD} waveform several times per clock cycle to extract more information from the signal than a simple DC level used in I_{DDQ} test [138][139]. Figure 17 shows the overview of this method called I_{DDF} testing. The basic theme is to sensitize a given path to make defects along the path alter the I_{DD} waveform and detect the alterations using frequency spectrum analysis. The first component harmonic is usually different for fault-free and faulty I_{DD} waveforms. Frequency spectrum analysis using an 8-point FFT was shown to be sufficient for detecting significant current waveform alterations caused by a defect [140]. Frequency domain analysis is shown to be useful in detecting single and multiple faults as well as distinguishing between different faults [141]. I_{DDF} testing has better immunity to noise than I_{DDQ} test, however, as I_{DD} frequency increases, higher sampling rates are required. Recent work suggests that it is possible to measure I_{DDT} up to about 1 GHz at test points close to the chip [142]. This requires expensive test equipment.

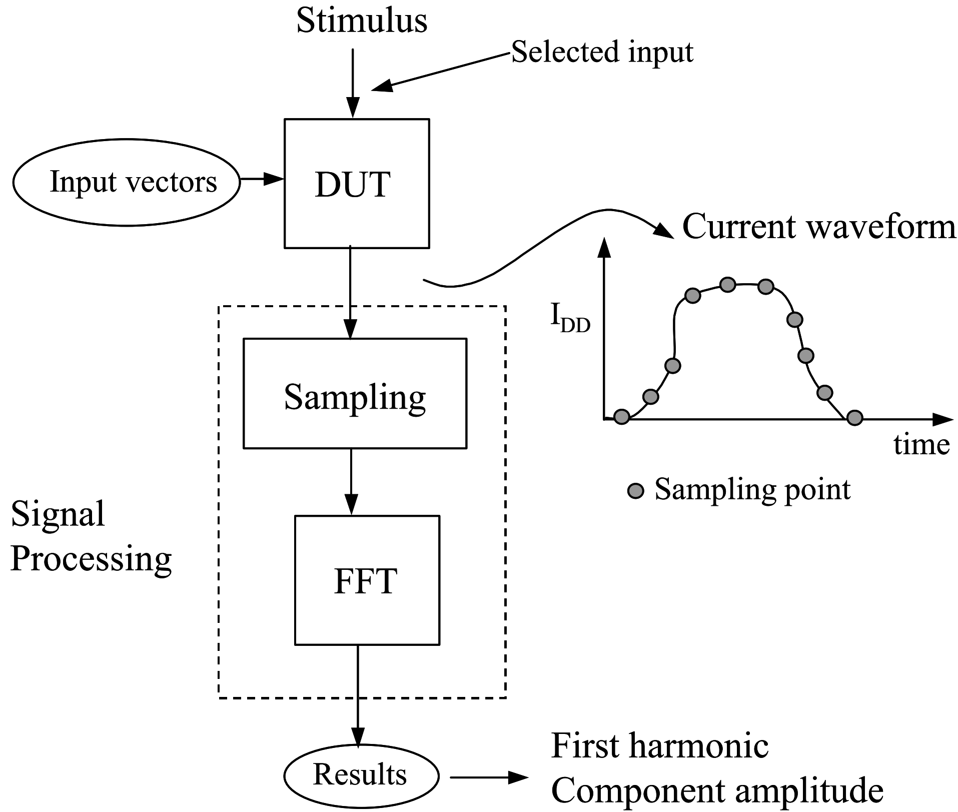

Fig. 17. Overview of I_{DDF} testing method.

7.5 Wavelet Transform-based Testing

Use of wavelet transforms for analysis of I_{DD} waveforms has been investigated [143][144]. The wavelet transform decomposes the I_{DDT} signal both in time and frequency domain. This property is useful for fault detection and localization. The wavelet transformation function (called *mother wavelet*) is oscillatory with energy confined to a finite interval. The continuous wavelet transform of a function *f(t)* with respect to a wavelet $\psi(t)$ is defined as:

$$W(a,b) = \int_{-\infty}^{\infty} f(t).\psi^{*}_{a,b}(t)\ dt \text{ where } \psi_{a,b}(t) = \frac{1}{\sqrt{|a|}}\psi\left(\frac{t-b}{a}\right)$$

Here a and b are real and * indicates complex conjugate. $W(a,b)$ is the transform coefficient of $f(t)$ for the given a, b. For a given a, $\psi_{a,b}(t)$ represents a shifted $\psi_{a,0}(t)$ by an amount b along time axis. If $a>1$, there is stretching of $\psi(t)$ while for $0<a<1$ there is a contraction of $\psi(t)$. The distinction between fault-free and faulty chips is achieved by comparing wavelet coefficient of the transient currents with those for the golden device for identical input. The wavelet-based fault localization depends on the mother wavelet used. The localization is effective if the occurrence of a fault in one module does not affect the current waveform in another module or power grid. The applicability of this method in real time is affected by sampling frequency. It is necessary to generate optimal test vectors for fault detection and localization.

7.6 Energy Consumption Ratio (ECR)

Recently the use of average dynamic currents for fault detection has been reported [145][146][147]. The advantage of this method is that average dynamic currents are easier to measure than rapid transient currents and it does not require high-speed measurement circuitry. ECR relies on the fact that a fault alters the number and location of signal transitions that occur due to a change in input. In other words, a fault can alter the energy consumed by the circuit. It uses two pairs of vectors, which are alternated at the input of the circuit. ECR is the ratio of currents (or energies) consumed by the two transitions. ECR is immune to process variations to the first order as the effect of process changes affects both the numerator and the denominator and gets canceled. To be effective, ECR requires a pair of vectors that maximizes the consumption ratio. That is, one vector that sensitizes the fault and the other that does not. This requires additional test vector generation effort. Like all other I_{DDX} methods, deciding the fault-free ECR threshold is not trivial. Use of statistical techniques like PCA has been shown to be useful [148].

8. FUTURE OF I_{DDX}-BASED TEST METHODS

As transistor geometries are scaled further, I_{DDQ} values and variation are projected to increase. For performance-optimized chips, leakage currents are expected to be in the range of 8 to 20 A by the year 2014 [56]. However, high-performance microprocessors already have leakage of similar magnitude. Increasing leakage not only makes I_{DDQ} test more difficult, but also increases static power dissipation. For mobile and battery-powered systems, it is crucial to keep leakage power as low as possible [56]. Increased static power dissipation also reduces reliability of a system due to increased temperature. This has fueled research for reducing the leakage current [55][149]. The reduction techniques are helpful in extending the usability of I_{DDQ} test to DSM chips.

Leakage reduction methods like Reverse Body Bias (RBB) [150][151], Multi-threshold CMOS (MTCMOS) [152] and transistor stacks [153] require circuit modification. MTCMOS and stacks require the selection of appropriate input vectors to reduce leakage [154] but otherwise do not fundamentally change I_{DDQ} test.

It is necessary to understand the components of the variation in I_{DDQ} in order to develop the most suitable screening method. Gate and sub-threshold leakage are dominating components of I_{DDQ}. Fowler-Nordheim (FM) tunneling increases as gate oxide thickness reduces. The ITRS lists the need to keep gate leakage to no more than 1% of the total leakage. The defective component of leakage current may fall as the supply voltage is scaled down. This would increase the overlap between faulty and fault-free I_{DDQ} distributions. As each I_{DDQ} technique loses its resolution, it will be necessary to combine them to screen defective I_{DDQ} values from defect-free ones. I_{DDQ} dependence on temperature, voltage, input pattern and correlation with parameters like flush delay or die position on a wafer must be exploited to define a multi-dimensional outlier identification method. Multi-parameter test strategies will be required in future [155]. Better electrical signatures to defect mapping will be needed to understand exact defect mechanisms [156]. Without this, the amount of yield loss/test escapes would be unacceptable.

I_{DDQ} test poses different challenges for low-power and high-performance chips. It appears that statistical analysis alone will be sufficient for low-power devices in the future. However, for high-performance chips the problem will need to be approached from several directions. The designers must attempt to make circuits I_{DDQ} testable by reducing background leakage as much as possible [157][158]. An accurate I_{DDQ} sensor is required [159]. The external current measurement using parametric measurement unit or similar methods is too slow and hence becomes impractical. A viable option is to use built-in current sensors (BICS) [160][161][162][163] that are embedded in a chip. The performance penalty for BICSs must be negligible. Research in producing faster, accurate and sensitive BICSs that have no or little performance penalty is needed [164]. For high-performance circuits, it will be necessary to partition [165][166] or power down the circuit [167] and embed multiple BICSs.

I_{DDQ} measurement must be supported by rigorous statistical data analysis to reduce yield loss in the future. Manufacturers must be able to define their own statistical procedures to optimally tune pass/fail criteria. It may not be possible to bin the chips until the data from a lot or wafer is collected. The trends in lot-to-lot or wafer-to-wafer variation in I_{DDQ} must be monitored and used in the analysis procedures. The use of inkless flows and electronic databases can support the post-process analysis. In some cases, it may be possible for testers to do on-the-fly calculations to enable a pass/fail decision. This will be more than simple comparison with a threshold. However, it has been suggested that for high-performance chips, testers cannot simply do pass/fail decision as it will lead to unjustifiable yield loss [168]. Hence, it will be necessary to take pass/fail decision making off the tester to off-line processing of test data.

I_{DDT} test methods are relatively new and except for ECR production test results are not available. These methods have yet to prove their value in production. New technologies increasingly use on-chip decoupling capacitors to handle the fast current transients. Such capacitors eliminate the high frequency information from the I_{DD} waveform, which may make the distinction between faulty and fault-free chips difficult. To what extent this will impact I_{DDT} test is unknown. The future of I_{DDT} test will depend on the availability of high-speed accurate sensors, measurement resolution and precision.

9. CONCLUDING REMARKS

In spite of all the efforts described here, I_{DDX} test will continue to lose its resolution to detect defects in the future. However, it will continue to remain a valuable component of the test suite. More research is required for reducing fault-free leakage, understanding new defect mechanisms to improve fault models [169] and to accurately predict defect levels for bulk CMOS technology with new materials and for new emerging technologies. New tests like VLV test [45] and $MINV_{DD}$ test [46][170] are potential alternatives to ensure IC quality and reliability. However, recent studies indicate that VLV can catch some defects detected by I_{DDQ} test, but cannot replace I_{DDQ} test [171]. Similarly, production test of ECR proves that it is more effective than VLV test [172]. With each technology advancement, all test methods lose their defect screening resolution. Hence, it will be necessary to combine several test methods for distinguishing outlier chips [173]. As advances in semiconductor technology pose greater challenges, I_{DDX} tests will continue to

evolve. Nevertheless, the feedback it provides for process control and improvement will remain extremely valuable for next generation technologies.

Table I. ITRS Projections for leakage currents of high-performance ICs [56]

Year	Maximum I_{DDQ} (mA)
2003	30 to 70
2005	70 to 150
2008	150 to 400
2011	400 to 1600
2014	8000 to 20000

Table II. Summary of I_{DDQ} Test Methods

Method	Features	Advantages	Disadvantages
I_{DDQ} vs. Temperature [66, 68]	Fault-free leakage current increases with temperature. Differences in leakage currents measured at two temperatures can distinguish faulty chips.	Simple	Low temperature measurement is too expensive. High temperature measurement may not be cost effective.
Delta I_{DDQ} [69, 93, 94, 96]	Differences (deltas) between two I_{DDQ} readings for consecutive vectors show near-zero mean and small variance for a fault-free chip.	Simple Ease of implementation.	Deciding fault-free variance is not easy Cannot screen passive and subtle active defects.
Current Ratios [103]	Ratio of maximum I_{DDQ} to minimum I_{DDQ} of fault-free chips is relatively constant.	Simple I_{DDQ} value need not be measured (comparison is enough).	Difficult to set low threshold for screening passive defects.
Statistical Clustering [101, 102]	Chips are grouped using statistical clustering method which groups data such that chips in a group have natural association with chips from the same group.	Inherently accounts for process variation.	Needs many readings for good clustering. Labeling clusters (faulty or fault-free) is difficult.
Statistical Outlier Rejection [107, 108]	Statistical outlier rejection methods are used for screening defective chips as they appear in the tail of distribution.	Simple Many outlier rejection methods are available.	Outliers affect the distribution properties. Data must be converted to standard distribution. Transformations can be hard to find. Threshold setting needs extensive empirical analysis.
Current Signature [87, 90]	Sorted I_{DDQ} values show steps or “jumps” for active defects and smooth signature for fault-free chips.	Simple, intuitive Considers intra-die variations.	Number of measurements determine screening resolution. Deciding fault-free step size is difficult. Cannot screen passive defects.
Eigen Signatures [106]	Relationship between mean I_{DDQ} and variance is explored to distinguish between faulty and fault-free chips, leakage variance is allowed to be proportional to the mean value.	Simple. Accounts for process variation.	Elaborate analysis may be needed. Outlier rejection treatment is subjective.
Principal Component Analysis (PCA) [123]	PCA is used to exploit the vector-to-vector correlation between chips using underlying process variation information.	Accounts for process variations.	Threshold setting is difficult.
Wafer-level correlation methods [115, 116, 119, 121]	Neighboring chips on the same wafer are used for estimating maximum fault-free I_{DDQ} to identify wafer-level “spatial outliers” (NNR, spatial fit, NCR, INDIT).	Accounts for process variation. No model building needed. Scaleable to new technologies.	Prior knowledge of wafer patterns may be necessary. Gross outliers must be rejected up front which requires threshold setting to identify “true” outliers.
I_{DDQ} Vs F_{max}/ Flush Delay [70, 72]	The fact that the fault-free leakage and delay or F_{max} are correlated is exploited to distinguish between faulty and fault-free chips.	Simple. Accounts for process variations.	May be applicable to mature, well-controlled processes only. Cannot do per-chip analysis.

Table III. Summary of I_{DDT} Test Methods

Method	Features	Advantages	Disadvantages
Pulse Response Testing (PRT) [126, 127]	Pulses both V_{DD} and V_{SS} power rails while applying fixed bias to input. Temporal and spectral analysis of I_{DD} is used to differentiate faulty and fault-free chips.	Test vector independent. Applicable to both digital and analog circuits.	May be impractical in production. Characterization and model building is difficult. Effectiveness falls for DSM technologies due to reduced supply voltage.
Dynamic Power Consumption Measurement [128, 132]	Integrate the I_{DD} value and convert to voltage, if voltage exceeds the threshold the chip is rejected.	Simple.	Slow. Does not account for process variations.
Transient Signal Analysis (TSA) [135, 136]	Uses multiple test points to sample I_{DD}. In the presence of a defect only I_{DD} sampled at test points closer to defect site are affected, thus distinguishing fault-free and faulty $I_{DD.}$	Accounts for process variation. Scaleable to new technologies.	Requires multiple test points.
Frequency Spectrum Analysis [134, 139, 140]	I_{DDT} waveform is sampled at multiple points. Harmonic analysis is used to differentiate between faulty and fault-free chips.	Insensitive to noise More robust and powerful technique.	Signal processing involved. Difficult and expensive for high-frequency chips.
Energy Consumption Ratio (ECR) [145, 146]	Applies a pair of vectors at the input and are alternated. The ratio of average currents (energies) consumed is used for screening.	Simple, insensitive to process variations.	Requires more test generation effort to maximize effectiveness Pass/fail threshold selection issue exists.

APPENDIX: SUMMARY OF THE SEMATECH EXPERIMENT S-121

The SEMATECH experiment S-121 was primarily conducted to evaluate the relative effectiveness of tests. The test vehicle used was a 116K gate 0.8 µm (0.45 µm L_{eff}) ASIC. Some portions of the chip operated at 40 MHz and others operated at 50 MHz. The device operated at 3.3 V and was I_{DDQ} testable i. e. had a minimal static leakage. A total of 18 466 dice on 75 wafers (5 lots) were tested at wafer probe and after packaging. The wafer level tests were conducted at 50°C while package tests were conducted at 25°C. In total four types of tests were performed. These include functional test, stuck-at scan test, delay test and an I_{DDQ} test. For the I_{DDQ} test a total of 195 test vectors were applied and 195 measurements were collected. This test used a pass/fail threshold of 5 µA. A timing measurement was performed by sending a transition from the scan-in pin to the scan-out pin of the scan chain and measuring the propagation delay (flush delay). The flush delay was used to establish relative performance for each device. A sample of packaged chips was subjected to six hours of BI following which all tests were performed. BI was dynamic and used 1.5X nominal V_{DD} at temperature of 140°C. A smaller sample was further subjected to 72 and 144 hours of extended BI. The findings revealed that all tests uniquely identified some defects. Several chips passed all tests but failed only I_{DDQ} test before and after BI. Conclusions drawn based on SEMATECH data are our own and do not necessarily represent the views of SEMATECH or its members companies.

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