A Circuit Level Fault Model for Resistive Bridges

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Delay faults are an increasingly important test challenge. Modeling bridge faults as delay faults helps delay tests to detect more bridge faults. Traditional bridge fault models are incomplete because these models only model the logic faults or these models are not efficient to use in delay tests for large circuits. In this paper we propose a physically realistic yet economical resistive bridge fault model to model delay faults as well as logic faults. An accurate yet simple delay calculation method is proposed. We also enumerate all possible fault behaviors and present the relationship between input patterns and output behaviors, which is useful in ATPG. Our fault simulation results show the benefit of at-speed tests.

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Additional Key Words and Phrases: bridge faults, fault models, delay faults

1. INTRODUCTION

Bridge faults are an important type of manufacturing defects [Rodriguez-Montanes et al.1992, Sar-Dessai and Walker 1999]. In order to generate test vectors that can achieve high fault coverage for bridge faults, it is important to have a realistic fault model for bridge faults.

Previous bridge fault models include logic fault models and delay fault models. Hao and McCluskey [1991] studied the effect of bridge faults inside of logic gates. Renovell et al. [1994; 1995] presented detailed electrical behavior for 0 Ω bridges and resistive bridges in CMOS devices. Chakravarty [1997] showed that the path-delay fault model is not adequate to model bridge faults. Sar-Dessai and Walker [1999] gave several logic fault models for resistive bridge faults. Moore et al. [2000] presented comprehensive delay fault analysis for resistive bridge models and cou-

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pling effects, but the delay calculation was not given. Other techniques, such as the mixed-mode simulation method by Chuang and Hajj [1993] and neural network techniques by Shaw et al. [2001], give more accurate bridge fault models. But these methods are not efficient for large circuits due to their high time complexity.

In this paper we propose a circuit level model for resistive bridge faults incorporating both logic and delay fault behaviors. A general closed form delay calculation method for bridge faults is proposed and the accuracy compared with SPICE is shown. All possible fault behaviors are illustrated and the relationship between input patterns and output behaviors, which is useful in ATPG, is presented.

Since modern VLSI circuits are interconnect dominant, this paper focuses on bridge faults between the interconnect. We do not consider feedback bridges, bridges between nets feeding the same gate, capacitive and inductive coupling, process variation, power supply and substrate noise [Krstic et al. 1999]. The delay of a net in this paper is defined as the time between the input of the driving gate reaches 50% Vdd and the input of the downstream driven gate reaches 50% Vdd.

The remainder of the paper is organized as follows. Section 2 describes the resistive bridge model, static and dynamic analysis and modeling procedures. Section 3 presents the application and Section 4 concludes with discussions.

2. FAULT MODEL

The objective of the resistive bridge fault model is to transform the effect of a resistive bridge fault to a logic fault or a delay fault, and to compute the delay change due to the bridge fault. We will first propose the circuit model, then perform static and dynamic analysis. Finally, we will give procedures to calculate the delay for the resistive bridge fault and present the relationship between input patterns and fault behaviors at outputs.

2.1 Circuit Model

The resistive bridge circuit model is shown in Figure 1. Each gate B_i is an arbitrary CMOS gate. To simplify the analysis, CMOS devices in B_1 and B_2 are replaced by switches and linear resistors in Figure 2, and B_3 and B_4 are replaced by buffers. We use a simple RC interconnect model that lumps interconnect parasitic capacitance with the load capacitance.

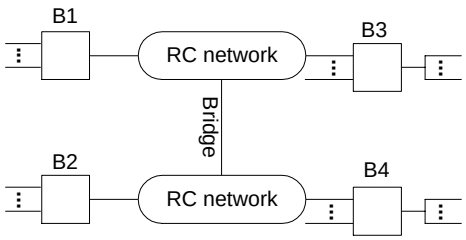


Fig. 1. The resistive bridge circuit model.

Circuit parameters in Figure 2 include pull-up and pull-down resistances R^1_{up}, R^1_{down} , R^2_{up} and R^2_{down} of B_1 and B_2, interconnect parasitic resistances R_1, R_2, R_3

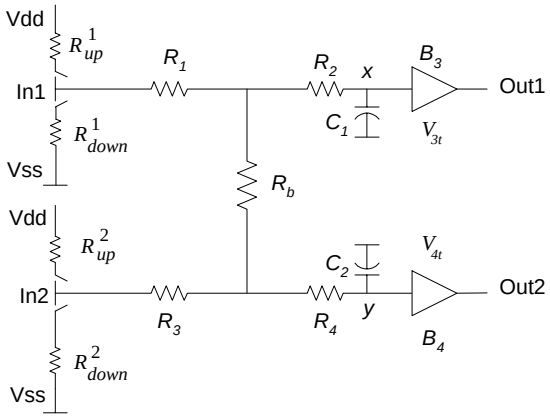


Fig. 2. The simplified resistive bridge circuit model.

and R_4, bridge resistance R_b, capacitances C_1 and C_2 that includes interconnect and sink capacitances, and logic interpretation voltages V_{3t}, V_{4t} of B_3 and B_4. The logic interpretation voltage V_t of a buffer is defined as follows. If the input of the buffer is below V_t, then the output is low. If the input of the buffer is above V_t, then the output is high. For inverters or other gate types, the definition is similar with some "high" and "low" exchanged. Inputs of B_3 and B_4 are denoted as x and y, respectively. For simplicity, the delay of Out1 (Out2) means the delay at x (y) in the whole paper.

2.2 Static Analysis

In the static analysis, it is assumed that input signals remain constant and output signals are stable. Therefore, all interconnect parasitic capacitances and sink capacitances are ignored.

There are four possible cases of input patterns in the static analysis. When In1 and In2 are both high, or both low, the bridge has no impact on the circuit. When In1 is low and In2 is high, the circuit is shown in Figure 3.

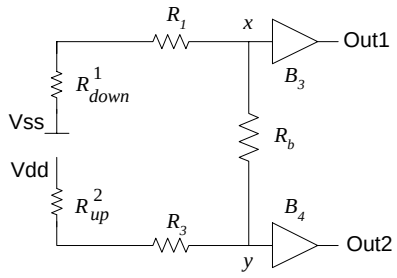


Fig. 3. The circuit model when In1 is low and In2 is high.

Define the Bridge Threshold Resistance (BTR) for input (high, low) for Out1 as

$$R_{1,Vss} = \frac{Vdd(R_1 + R^1_{down})}{V_{3t}} - (R_1 + R_3 + R^1_{down} + R^2_{up}). \quad (1)$$

When $R_b < R_{1,Vss}$, the voltage at x is greater than V_{3t} and Out1 is high, which is a logic fault. When $R_b > R_{1,Vss}$, there is no logic fault, but there might be an increased delay, which is discussed in the section 2.3. The relationship between Out1 and R_b is illustrated in Figure 4.

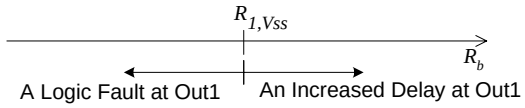


Fig. 4. The relationship between R_b and Out1.

Similarly for Out2, the BTR is

$$R_{2,Vdd} = \frac{V_{4t}(R_3 + R^2_{up})}{Vdd - V_{4t}} - (R_1 + R^1_{down}). \quad (2)$$

The case when In1 is high and In2 is low is symmetric. The corresponding BTRs are given as follows.

$$R_{1,Vdd} = \frac{V_{3t}(R_1 + R^1_{up})}{Vdd - V_{3t}} - (R_3 + R^2_{down}), \quad (3)$$

$$R_{2,Vss} = \frac{Vdd(R_3 + R^2_{down})}{V_{4t}} - (R_1 + R_3 + R^2_{down} + R^1_{up}). \quad (4)$$

It is known that for Boolean functions with two inputs, only four are monotone and non-constant. Therefore, the behavior of Out1 in Figure 2 can only be one of the four in Figure 5. Table I summarizes the above analysis and shows which model the circuit behaves. The concept of Bridge Threshold Resistance is similar to the concept of critical (limit, detectable) resistance studied in previous work [Renovell et al. 1995, Sar-Dessai and Walker 1999, Moore et al. 2000]. In this paper, simple formulas to compute BTRs are presented.

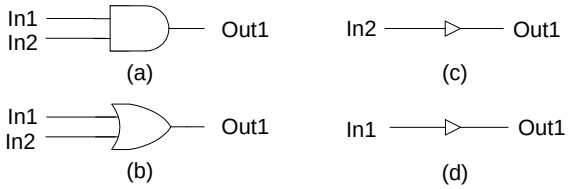


Fig. 5. Four basic resistive bridge fault models for the static analysis.

Table I. The Bridge Fault Model for Out1.

R_b range	Out1 Model
$R_b \leq min(R_{1,Vdd}, R_{1,Vss})$	(c)
$R_{1,Vss} < R_b < R_{1,Vdd}$ (if $R_{1,Vss} < R_{1,Vdd}$)	(a)
$R_{1,Vdd} < R_b < R_{1,Vss}$ (if $R_{1,Vdd} < R_{1,Vss}$)	(b)
$R_b \geq max(R_{1,Vdd}, R_{1,Vss})$	(d)

Some useful properties can be derived directly from the models. For example, it is impossible for all BTRs to be greater than zero. Here is a simple proof. If all BTRs are set to be greater than zero, then from equations (1) and (2), we can derive that $V_{4t} > V_{3t}$. Similarly, from equations (3) and (4), we can derive that $V_{3t} > V_{4t}$, which is a contradiction. Therefore, all BTRs cannot be greater than zero (or less than zero with a similar proof) at the same time. Thus, Out1 and Out2 cannot behave as the model shown in Figure 5(c) simultaneously, i.e. there exist some input vectors that make logic values of two outputs not be swapped. When $R_b < max(R_{1,Vdd}, R_{1,Vss}, R_{2,Vdd}, R_{2,Vss})$, Out1 and Out2 cannot behave as the model shown in Figure 5(d) simultaneously, i.e. there must be a logic fault at either Out1 or Out2.

2.3 Dynamic Analysis

In the dynamic analysis, there are four types of input signals: high, low, rising (from low to high), and falling (from high to low). According to the static analysis, the output behavior eventually settles down to one of the four fault models in Figure 5, determined by BTR values. There are totally 16 cases of input type combinations for In1 and In2. The analysis for all cases is similar to the following case.

Consider the case when In1 is rising and In2 is low. The circuit in Figure 2 can be simplified to the circuit in Figure 6. If $R_b \leq R_{1,Vdd}$, the static analysis shows that there is a logic fault for Out1, which can be detected by logic tests. If $R_b > R_{1,Vdd}$, there is no logic fault.

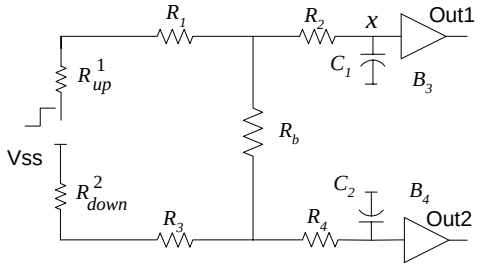


Fig. 6. The circuit model when In1 is rising and In2 is low.

From the circuit analysis by matching the second moment of transfer function [Pillage and Rohrer 1990], we found that when there is a rising input on In1, the behavior of x in Figure 6 can be approximated by the behavior of x in Figure 7,

where

$$C_e = C_1 + \frac{(R^2_{down} + R_3)^2}{(R^2_{down} + R_3 + R_b)^2} \cdot \frac{C_2}{1 + |R_4 - R_2| / (R^1_{up} + R_1 + R_2)}.$$

The coefficient $\frac{1}{1 + |R_4 - R_2| / (R^1_{up} + R_1 + R_2)}$ is got experimentally to balance the interconnect resistance R_4 and R_2. When $R_4 = R_2$, the following fact is true: the first two moments of driving admittance [O'Brien and Savarino 1989] in Figure 6 and 7 are the same, which is

$$\frac{1}{R^2_{down} + R_3 + R_b + R^1_{up} + R_1} + \frac{(R^2_{down} + R_3)^2 C_2 + (R^2_{down} + R_3 + R_b)^2 C_1}{(R^2_{down} + R_3 + R_b + R^1_{up} + R_1)^2} s + \mathrm{O}(s^2).$$

In the approximation, B_3 is only regarded as a sink capacitance that is included in C_1 in Figure 6 and C_e in Figure 7.

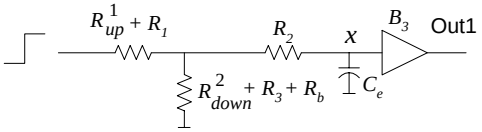


Fig. 7. The approximation circuit model for Out1 when In1 is rising and In2 is low.

In Figure 6, if the bridge does not exist in the circuit, then the equivalent circuit is shown in Figure 8(a), where $R_{line} = R_2 + R_1 + R^1_{up}$.

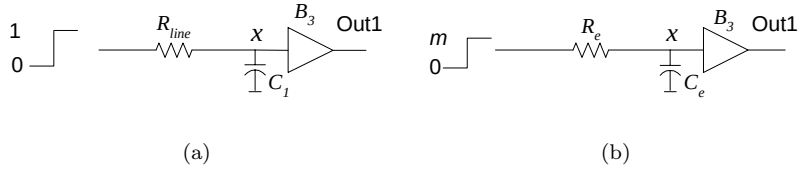


Fig. 8. (a) The equivalent circuit of Figure 6 when there is no bridge. (b) The equivalent circuit of Figure 7.

Define the delay at x in Figure 8(a) as d_1, then

$$d_1 = -R_{line} \cdot C_1 \cdot \ln(0.5). \tag{5}$$

Similarly, the equivalent circuit of Figure 7 is shown in Figure 8(b), where

$$\begin{aligned} R_e &= R_2 + (R_1 + R^1_{up}) // (R^2_{down} + R_3 + R_b), \\ m &= \frac{R^2_{down} + R_3 + R_b}{R_1 + R^1_{up} + R^2_{down} + R_3 + R_b}. \end{aligned}$$

Here, $(R_1+R^1_{up})//(R^2_{down}+R_3+R_b)$ gives the parallel resistance of two resistances. Define the delay at x in the Figure 8(b) as d_2, then we can get

$$d_2 = -R_e \cdot C_e \cdot \ln\left(1 - \frac{0.5}{m}\right). \tag{6}$$

Since the peak voltage at x in Figure 8(b) is only a fraction of Vdd, there is an increased delay at Out1. Intuitively, m can be seen as the voltage division ratio, and R_e can be seen as the effective resistance from upstream to x. When $R_b \to \infty$, $C_e = C_1$, $R_e = R_{line}$, $m = 1$ and $d_2 = d_1$.

From equations (5) and (6), the increased delay $d' = d_2 - d_1$ can be computed as

$$\begin{aligned} d' &= \left(a \cdot b \cdot \frac{\ln(1 - \frac{0.5}{m})}{\ln(0.5)}\right) \cdot d_1 \\ &= \left(-a \cdot b \cdot \log_2\left(1 - \frac{0.5}{m}\right)\right) \cdot d_1, \end{aligned} \tag{7}$$

where $a = \dfrac{C_e}{C_1}$, $b = \dfrac{R_e}{R_{line}}$. In the equation (7), a can be seen as the ratio between the effective capacitance with and without the bridge, b can be seen as the ratio between the effective resistance with and without the bridge. When the input pattern is (falling, low), then $d' = (-a \cdot b \cdot \log_2(0.5/m)) \cdot d_1$, where all parameters have similar meanings to parameters in (rising, low) case except for different values. Generally, if the initial voltage value of a rising input in Figure 8(b) is defined as g, the static value after the dynamic process is defined as h, then

$$d' = \left(-a \cdot b \cdot \log_2\left(1 - \frac{0.5 - g}{h - g}\right)\right) \cdot d_1 = \left(-a \cdot b \cdot \log_2\left(\frac{0.5 - h}{g - h}\right)\right) \cdot d_1. \tag{8}$$

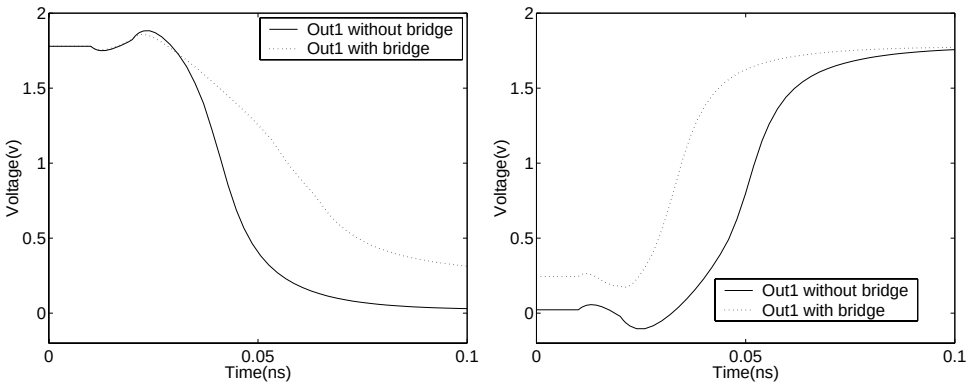
If the initial value of a falling input is g, the static value after the dynamic process is h, it is interesting that d' can be written in the same format as in the rising case except for different parameter values.

In the equation (8), we write d' as the function of d_1 since we can calculate d' from d_1 which is a more accurate value such as the delay including the cell delay from SPICE simulation or delay tables. Our equation can also be easily modified when there is a ramp input in Figure 6. We can abstract the ramp input by a step input applied at the instant when the ramp crosses the 50 % point and an extra delay $\tau/2$, where τ is the slope of the ramp input [Kashyap et al. 2000]. Now the equation (8) is modified to

$$d' = \frac{(-a \cdot b \cdot \log_2(\frac{0.5-h}{g-h}))}{1 + \frac{\tau/2}{-R_{line} \cdot C_1 \cdot \ln(0.5)}} \cdot d_1. \tag{9}$$

Through SPICE simulation the bridge resistance can increase or decrease the delay (d' can be greater or less than zero) depending on input patterns. This was also mentioned in previous work [Moore et al. 2000]. Figure 9 is the SPICE simulation of two interconnect segments from the layout of the ISCAS85 circuit c432. The bridge resistance is 1 KΩ. There is an increased delay at Out1 when input pattern (In1, In2) is (falling, high), and a decreased delay at Out1 when the

input pattern is (rising, high). The decreased delay may cause a hold time violation or race at Out1. This type of fault cannot be detected by the current delay test.



(a) (b)

Fig. 9. (a) A bridge causes an increased delay at Out1 when input pattern is (falling, high). (b) The bridge causes a decreased delay at Out1 when input pattern is (rising, high).

2.4 Modeling Procedure

Based on the above analysis, we derive the bridge fault model as follows. All logic and delay faults are included in the model. Previous fault models such as the aggressor-victim model [Moore et al. 2000] are special cases of this model.

(1) Compute R^1_{up}, R^1_{down} , R^2_{up} , R^2_{down} , V_{3t} and V_{4t} from the cell library and the input pattern for cells other than inverter/buffers. Compute R_1, R_2, R_3, R_4, C_1 and C_2 from the interconnect parasitics.

(2) Compute BTR values $R_{1,Vdd}$, $R_{1,Vss}$, $R_{2,Vdd}$ and $R_{2,Vss}$ according to equations (1) to (4).

(3) For the fault simulation, R_b is given. Use R_b to choose a fault model from Figure 10 according to Table I. When there is a delay fault, compute

$$d' = (-l \cdot \log_2((0.5 - h)/(g - h)) - 1) \cdot d_1, \tag{10}$$

where d_1 is the nominal delay of Out1, l, g and h are chosen according to Table II.

In Table II, behaviors at Out1 for Figure 10(d) with all input patterns are presented. If both In1 and In2 change, it is assumed that two inputs change simultaneously. If two inputs do not change simultaneously, we treat the case as the combination of two cases happening sequentially. For example, if both inputs are rising and In1 is faster, then this case is consistent with the combination of (r, 0) and (1, r).

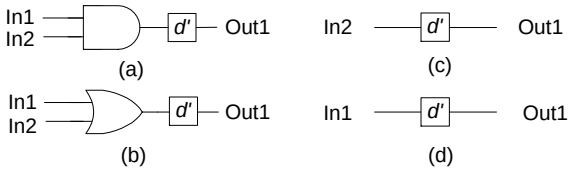


Fig. 10. Four basic resistive bridge fault models.

Table II. Increased delay(ID) or decreased delay (DD) at Out1 for Figure 10(d), r means rising, f means falling, 1 means high, 0 means low, and other variables are defined in equation series (11).

Input Pattern (In1, In2)	Out1 behavior for Figure 10(d)
Both static (0, 0) , (0, 1), (1, 0), (1, 1)	No ID nor DD
Same direction (r, r), (f, f)	
In1 static (0, r), (0, f), (1, r), (1, f)	
(r, 0)	ID, $g = 0$, $h = m_1$, $l = a_1 \cdot b_1$
(f, 0)	DD, $g = m_1$, $h = 0$, $l = a_1 \cdot b_1$
(r, f)	ID or DD, $g = m_2$, $h = m_1$, $l = a_1 \cdot b_1$
(f, r)	ID or DD, $g = m_1$, $h = m_2$, $l = a_2 \cdot b_2$
(r, 1)	DD, $g = m_2$, $h = 1$, $l = a_2 \cdot b_2$
(f, 1)	ID, $g = 1$, $h = m_2$, $l = a_2 \cdot b_2$

Some constants in Table II are given as follows. Constants a_i's, b_i's and m_i's have similar meanings to those explained above.

$$a_1 = 1 + \frac{(R^2_{down} + R_3)^2}{(R^2_{down} + R_3 + R_b)^2} \cdot \frac{C_2/C_1}{1 + |R_4 - R_2| / (R^1_{up} + R_1 + R_2)},$$

$$a_2 = 1 + \frac{(R^2_{up} + R_3)^2}{(R^2_{up} + R_3 + R_b)^2} \cdot \frac{C_2/C_1}{1 + |R_4 - R_2| / (R^1_{down} + R_1 + R_2)},$$

$$b_1 = \frac{R_2 + (R_1 + R^1_{up})//(R^2_{down} + R_3 + R_b)}{R^1_{up} + R_1 + R_2},$$

$$b_2 = \frac{R_2 + (R_1 + R^1_{down})//(R^2_{up} + R_3 + R_b)}{R^1_{down} + R_1 + R_2},$$

$$m_1 = (R^2_{down} + R_3 + R_b)/(R_1 + R^1_{up} + R^2_{down} + R_3 + R_b),$$

$$m_2 = (R^1_{down} + R_1)/(R_1 + R^1_{down} + R^2_{up} + R_3 + R_b). \quad (11)$$

For other models in Figure 10, the same delay formula can be used to compute the increased or decreased delay, except for some input vectors causing logic faults at Out1. Similar results for Out2 can be easily derived from Figure 10 and Table II by replacing Out2 with Out1, input pattern (In2, In1) with (In1, In2), $R_{2,Vdd}$ with $R_{1,Vdd}$ and $R_{2,Vss}$ with $R_{1,Vss}$. All the equations in (10) and (11) need to be recomputed by exchanging all the superscript 1 with 2, R_3 with R_1, R_4 with R_2 and C_1 with C_2 in the right hand side. For example, when input pattern (In2, In1)

is (r, 0),

$$a_1 = 1 + \frac{(R^1_{down} + R_1)^2}{(R^1_{down} + R_1 + R_b)^2} \cdot \frac{C_1/C_2}{1 + |R_4 - R_2| / (R^2_{up} + R_3 + R_4)}.$$

When the input is a ramp signal, the modeling procedure is same except the delay formula (10) needs to be modified in the way shown in section 2.3. We use "Step input delay model" and "Ramp input delay model" to distinguish two different formulas, though in real applications only one formula is needed and the effect of the ramp input is considered as one coefficient.

Since driving resistances are dependent on input patterns for cells other than inverters/buffers, in the static fault simulation in which input patterns are unknown, resistances are chosen to maximize (minimize) the delay effect that gives optimistic (pessimistic) estimation.

In Table II, there are two input patterns, (r, f) and (f, r), which may cause an increased delay or a decreased delay at Out1 and Out2 simultaneously. However, it can be easily derived from equation series (10) and (11) that the delay of Out1 with input (r, 0) is greater than the delay with input(r, f), and the delay with input (f, 1) is greater than the delay with input (f, r). Therefore, to maximize the delay of Out1, the best input patterns are **(r, 0)** and **(f, 1)**. Whether the former is better or the latter is better depends on the parameters. To maximize the delay of Out2, the best input patterns are **(0, r)** and **(1, f)**. Similarly, to minimize the delay at Out1, the best input patterns are **(r, 1)** and **(f, 0)** and to minimize the delay at Out2, **(1, r)** and **(0, f)**. To maximize or minimize the delay at both output simultaneously, the best input patterns may be **(r, f)** and **(f, r)**. Also, the delay formula we derived helps to choose input patterns at the previous stage. As shown in Figure 11, when the output of B_1 is rising, and the output of B_2 stays low, then there will be an increased delay. There are three input patterns, (1, f), (f, 1) and (f, f), which set the output of B_1 to a rising signal. However, (f, f) will produce less delay than the other two patterns since it decreases the pull-up resistance. Therefore, we should choose best patterns at previous stage to maximize or minimize the driving resistance.

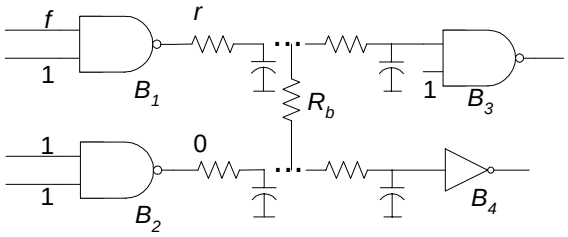


Fig. 11. Example circuit for simulation.

For cases (r, 0) and (f, 1), simulation results of SPICE and our delay model on the example circuit in Figure 11 with the step input are shown in Figure 12 and Figure 13. In Figure 11, the input vector assignment for (r, 0) is shown. The technology

is TSMC 180 nm 1.8 V. The PMOS size (width/length) is 540nm/180nm, and the NMOS size is 270 nm/180 nm. Pull-up/down resistances range from 1.5 KΩ to 3.2 KΩ, which are computed based on the linear region CMOS U-I curve [Weste and Eshraghian 1993]. Sink capacitances are 2.2 fF and 3.1 fF for the inverter and NAND gate, respectively. The logic interpretation voltage is 0.9 V. There are 8 RC segments in each interconnect (same for the two lines), in which the total resistance is 17.4 Ω and the total capacitance is 4 fF. The bridge locates in the middle of the two nets. BTRs $R_{1,Vss}$ for Out1 is greater than zero and $R_{1,Vdd}$ is less than zero. Out1 can only behave as the model in Figure 10(d) or (b) based on Table I.

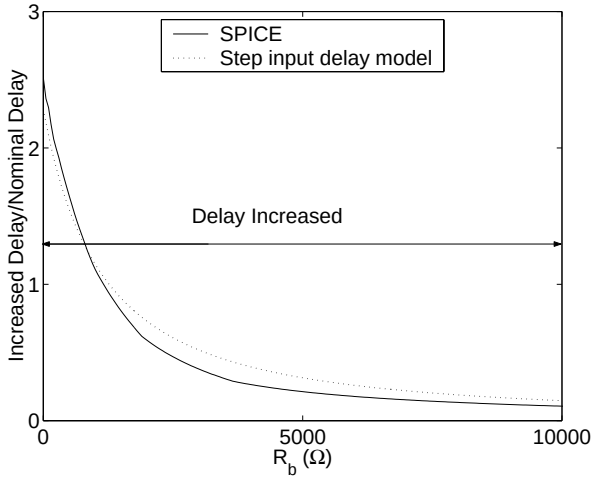


Fig. 12. An example relationship between R_b and the increased delay at Out1 with the rising step input.

When $R_b > R_{1,Vss}$, in both Figure 12 and Figure 13, Out1 behaves as Figure 10(d) and an increased delay exists. Bridge faults falling in this range may be detected by delay tests with our fault model, but may not be detected by traditional logic tests with infinitely slow speed.

When $R_b \leq R_{1,Vss}$, Out1 behaves as Figure 10(b) in both figures but appears as an increased delay in Figure 12 and a logic fault in Figure 13. In this case, even though there is a delay fault for Out1 with some input patterns, bridge faults in this range can still be detected by traditional logic tests with other input patterns. Both delay and logic tests may detect these bridge faults.

For the case (r, 0), simulation results on the example circuit with the ramp input are shown in Figure 14. The slope of the ramp input is 0.01ns, which is almost half of the nominal delay of Out1. Results of SPICE, step input delay model and ramp input delay model are compared and we can see that the ramp input delay model considering the slope effect gives more accurate result when R_b increases.

From all figures, our model shows a good match with SPICE simulation results. However, there are still some errors, which come from following sources: cell delay errors due to the linear resistance model and lumped capacitance model for driving

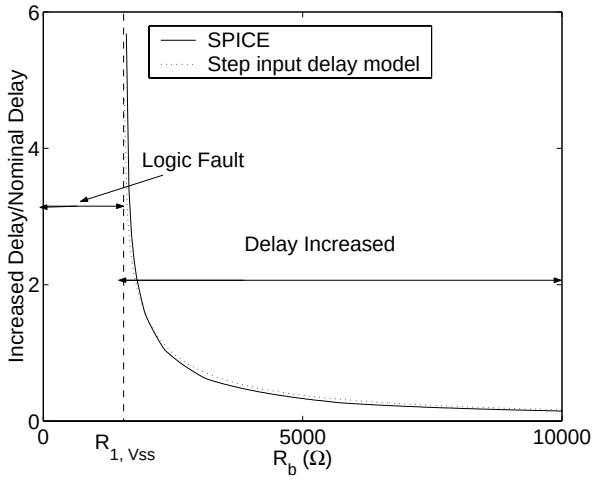


Fig. 13. An example relationship between R_b and the increased delay at Out1 with the falling step input.

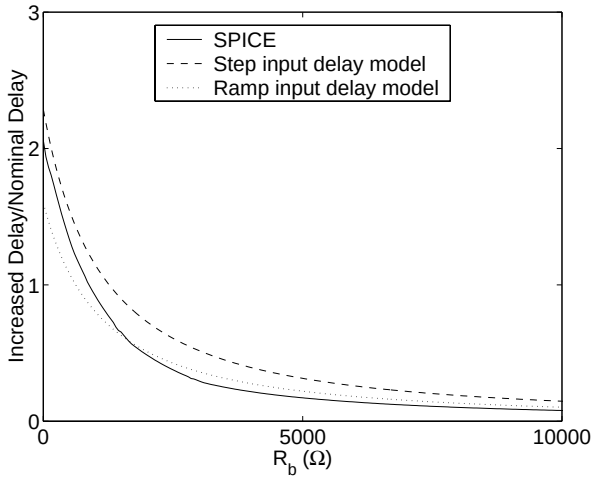


Fig. 14. An example relationship between R_b and the increased delay at Out1 with the rising ramp input.

gates, and interconnect errors due to simple RC interconnect and the approximation from Figure 6 to Figure 7.

In our experiment, when the bridge location is not in the middle of the two nets, the average delay varies by 0.1%. In general, if we do not know the exact location of a bridge, we will assume it locates in the middle of the two nets. It is a good approximation in practice. Some previous work also showed that the delay effect of a bridge fault has little relation with its location [Irajpour et al. 2003].

3. APPLICATION

The resistive bridge model developed in this paper has been implemented in the CodSim delay fault simulator [Qiu et al. 2003]. In the experiments, the bridge sites are assumed to be between two nets where large coupling capacitances exist. Such net pairs can be extracted using commercial capacitance extraction tools. The ISCAS85 benchmark circuits are used and the circuit layout is done with the Cadence Silicon Ensemble in TSMC 250 nm 3 V 3-metal technology. Commercial parasitic extraction tools are used to extract parasitics and compute net delays. The logic interpretation voltages are from 1.4 V to 1.5 V, and pull-up/down resistances of all gates are from 1 KΩ to 4 KΩ. For multi-input gates, pull-up/down resistances are computed assuming only one input changes at any time. The clock period is set to be 5% longer than the delay of the longest structural path.

Table III shows the simulation results for the ISCAS85 circuits, using 10 000 random vectors. Circuit c2670 is not included due to a parasitic extraction tool problem. The bridge resistance is approximately uniformly distributed from 0 Ω to 40 KΩ [Spica et al. 2001]. Columns 3 and 4 show the fault coverage using full-speed and half-speed tests, respectively. The fault coverage is computed by averaging the detected bridge resistance range over the potentially detectable resistance range for each bridge site. The half-speed tests can be considered fast logic tests and the full-speed tests can be considered the at-speed built-in self-tests (BIST), whose fault coverage is 1-5% higher than the half-speed tests. Using our model, for the first time it becomes possible to estimate the benefit from at-speed tests for resistive bridge faults. Our model is independent of the bridge resistance distribution, and therefore more accurate fault coverage can be computed if a more accurate distribution is known. Column 6 shows the simulation time and indicates that our bridge model is computational efficient.

Table III. Delay fault simulation results for 10 000 random vectors using our bridge model.

Circuit	Total Bridges	Resistive Bridge Model FC (%)		Sim.
		Full-Speed	Half-Speed	Time (s)
c432	821	88.1	84.4	1.4
c499	1,102	93.5	89.4	2.2
c880	1,412	90.0	86.2	2.4
c1355	2,488	88.6	84.2	7.0
c1908	4,007	92.0	91.9	5.1
c3540	8,919	87.0	86.7	17.9
c5315	12,168	94.3	94.0	18.6
c6288	14,170	91.6	91.4	22.5
c7522	12,156	87.2	86.6	25.7

4. CONCLUSIONS

In this work we have described physically realistic bridge fault models incorporating both logic and delay effects of bridge faults. We propose a closed form delay calculation method for bridge faults with step and ramp inputs. All fault behaviors are illustrated and input patterns targeting specific fault behaviors are presented. Experimental results show our delay calculation is accurate and efficient. The new

fault model and the fault coverage metric have been used in our CodSim simulator tool whose results show the benefit of at-speed tests.

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