I_{DDQ} Test Using Built-In Current Sensing of Supply Line Voltage Drop

Bin Xue, D. M. H. Walker

Dept. of Computer Science
Texas A&M University
College Station TX 77843-3112
Tel: (979) 862-4387
Email: {binxue, walker}@cs.tamu.edu

Abstract

A practical built-in current sensor (BICS) is described that senses the voltage drop on supply lines caused by quiescent current leakage. This non-invasive procedure avoids any performance degradation. The sensor performs analog-to-digital conversion of the input signal using a stochastic process, with scan chain readout. Self-calibration and digital chopping are used to minimize offset and low frequency noise and drift. The measurement results of a 350 nm test chip are described. The sensor achieves a resolution of 182 μA, with the promise of much higher resolution.

1. Introduction

Quiescent current (I_{DDQ}) testing is widely used to screen out many defects that escape conventional test method [1][2] and therefore it becomes a powerful complement to conventional testing methods. Besides testing, I_{DDQ} is also very useful in defect diagnosis [3]. However the future of I_{DDQ} testing is uncertain as leakage currents continue to rise. The International Technology Roadmap for Semiconductors projects that I_{DDQ} levels and variation will rise rapidly with each technology generation, making it harder to differentiate the I_{DDQ} levels of a faulty and faulty-free circuit [4][5]. Built-in current sensors (BICS) have been proposed both to speed up I_{DDQ} testing and to increase its resolution by virtually partitioning the supply mesh, so that each partition has a relatively small defect-free I_{DDQ} level [6][7]. However most BICS designs proposed to date have certain drawbacks, including large area overhead, chip speed penalty, high power supply voltage, substrate current injection, or limited BICS locations [8][9][10][11][12][13][14]. As a result, BICSs have rarely been used in production.

Our previous work using a MAGFET sensor in a BICS had a relatively low signal-to-noise ratio (SNR) and high calibration drift [15]. The proposed BICS is based on sensing the voltage drop on the supply lines caused by the I_{DDQ} current. This approach was first used by van Lammeran [16], using an analog approach. Sunter proposed a related scheme using the 1149.4 analog bus [17]. These approaches do not scale to large numbers of sensors. We previously developed a voltage drop BICS, but it suffered from low calibration resolution [18]. In view of these shortcomings, we propose a more robust BICS design, which has the advantage of small area, low power, no chip speed penalty and it can be used for practical I_{DDQ} testing and diagnosis of large, high-performance chips.

The organization of this paper is as follows. The detailed sensor system design is described in section 2. The experimental test chip result is presented and discussion is given in section 3. The conclusions and future work are described in section 4.

2. I_{DDQ} Sensor System Description

The proposed BICS is designed to sense I_{DDQ} by measuring the voltage drop through the resistance of a short section of a V_{DD} line. With slight modification it can be used to sense a ground line. The power line segment must be short enough to permit convenient tapping without requiring long and potentially noisy tap wires, and without interfering with the power grid design. For instance, ten squares of V_{DD} line with a sheet resistance of 10 mΩ/□ will generate a 1 μV signal when the current is 10 μA. We will use 1 μV as our desired signal resolution.

Since the tap wires have insignificant capacitance and current, the BICS does not introduce a performance penalty, unlike BICSs that introduce a series impedance. The BICS is fully digital and consumes little power in operation, and only leakage power when idle. The signal is digitized using a self-calibrated stochastic sensor, which can be read out via a scan chain. These characteristics are essential if large numbers of sensors are to be used on a chip [19].

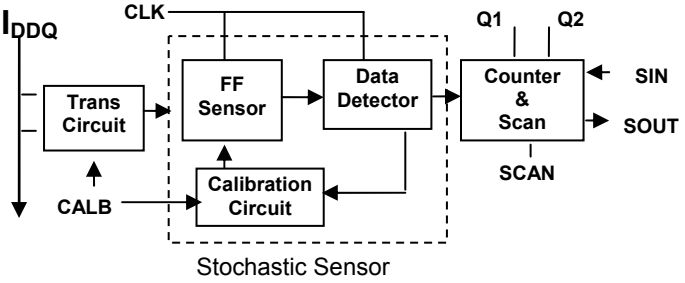

Figure 1. Block diagram of the I_{DDQ} Sensor.

The block diagram of the BICS is shown in Figure 1. The major BICS components are the flip-flop (FF) sensor, calibration circuit, and counter/scan chain. The BICS system works as follows. The signal passes through the transmission circuit and into the stochastic sensor. The stochastic sensor amplifies the small signal and resolves into either "1" or "0" in each clock cycle. The probability of resolving into each state is determined by the SNR. The data detector converts this flip to a counter clock pulse in measurement mode and calibration pulses in calibration mode. The generated bit stream of "0" and "1" is then accumulated in the counter. The counter value is the digital representation of the signal, so the stochastic sensor and counter form an analog-to-digital converter (ADC). The counter results can be scanned out. The self-calibration circuit nulls out any circuit imbalance and low frequency noise. The stochastic approach has two advantages: an ADC can be implemented in a small area

using digital components, and it can measure a signal much smaller than the random noise by operating in the metastable region. The design and functionality of each sensor components are elaborated in the following sections.

2.1. Transmission Circuit

The transmission circuit shown in Figure 2 has two roles. During measurement, it forms a low-pass filter between the input signal and flip-flop. During calibration, the inputs are disconnected and the outputs shorted and connected to V_{DD}. Inputs ina/inb feed pass transistors P0/P1 to outputs outa/outb. NMOS transistors N0/N1 are used as capacitors to form low-pass filters in combination with P0/P1. Transistors P0/P1 are turned off and the outputs are clamped to V_{DD} by P4/P5 and equalized by P3 during calibration. This permits calibration immediately prior to sensing, greatly reducing the drift requirements of the calibration circuit. The devices are larger than the technology minimum to reduce mismatch and noise. The circuit is designed to sense the V_{DD} line, but can be readily redesigned to sense the ground line. Sensing both V_{DD} and ground can reduce the number of sensors required [19].

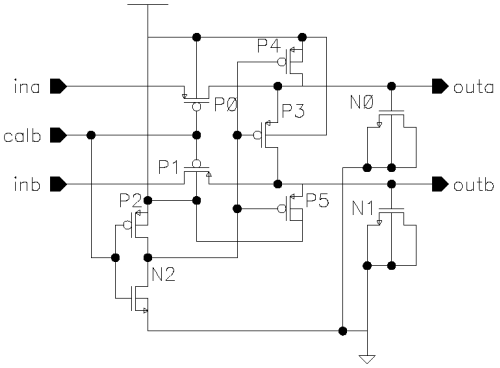

Figure 2. Transmission circuit.

2.2. Flip-Flop Stochastic Sensor

The flip-flop stochastic sensor is shown in Figure 3. When transistor P8 is turned off (clk is high), output nodes outn and outp are pulled to GND through inn/inp and igate_p/igate_n. When P8 is turned on, the differential input signal inp/inn is amplified with pulldown transistors N1/N4 in series with calibration transistors N5/N6, working against pullup transistors P6/P7. The flip-flop nodes integrate the input signal until the cross-coupled pulldown transistors N2/N3 turn on, comparing the signal to the noise, and positive feedback results in a flip-flop decision.

The response of a stochastic sensor follows a Gaussian cumulative density function (CDF) around the metastable point [20][21]. This can be approximated as linear when the signal is much smaller than the noise, as shown in Figure 4. The probability of getting a "0" or "1" from the flip-flop represents the equivalent magnitude of the analog input signal. The sign relative to 0.5 indicates the direction of I_{DDQ} flow. Since the CDF slope falls with rising noise amplitude, the "gain" of the stochastic sensor is inversely proportional to the noise. The noise has zero mean, so does not introduce an offset. The stochastic sensor achieves high sensitivity and high noise immunity through repetitive operation. Outputs of the stochastic sensor decisions, outn/outp, are fed into a counter. Using the slope of the CDF, the magnitude of the input can be deduced from the counter value.

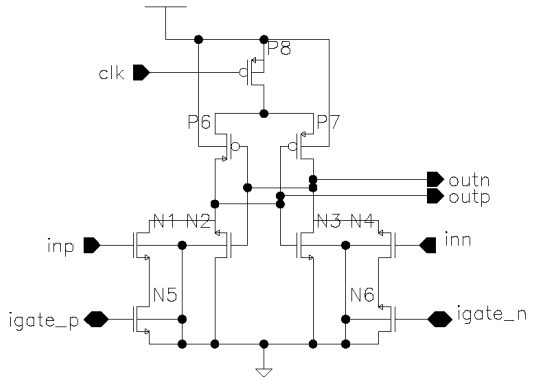

Figure 3. Flip-Flop Stochastic Sensor

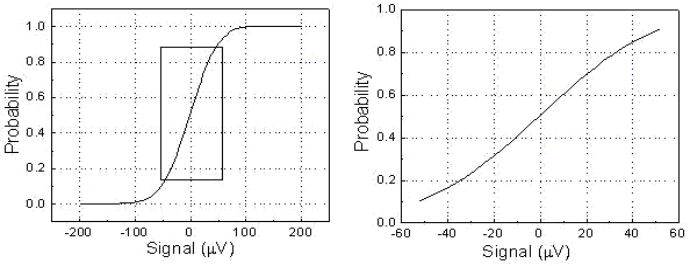

Figure 4. Stochastic sensor conceptual transfer curve. The transfer curve is approximately linear when the signal is much smaller than the noise.

The predicted sampling variance is [22]:

$$\frac{pq}{N} \sim \frac{0.25}{N}$$

and the standard deviation is:

$$\sigma = [pq/N]^{\frac{1}{2}} \sim \frac{0.5}{\sqrt{N}}$$

where N is the number of measurement cycles and p and q are the probability for either side of the stochastic sensor to get a "1". This is close to 0.5 for our application. The probability for a "1" decision is given by:

$$p \sim 0.5 \pm \frac{1}{\sqrt{2\pi}} \int_0^S \exp^{-1/2u^2}\, du$$

$$p \sim 0.5 \pm \frac{s}{\sqrt{2\pi}}$$

where s is the signal to noise ratio. So we have:

$$N \cdot p \sim N \cdot 0.5 \pm \frac{N \cdot s}{\sqrt{2\pi}}$$

The flip-flop noise comes from external noise and transistor noise. The transistor has two sources: thermal noise (white noise) and flicker noise [23], defined as follows:

$$S_{IW} = \begin{cases} \frac{4kT}{R_{FET}} & \text{ohmic region} \\ \frac{8kTg_m}{3} & \text{saturation} \end{cases} \qquad S_{If} = \frac{2K_f K' I_{DQ}}{C_{OX} L^2 f}$$

where S_{IW} and S_{If} define the white noise and flicker noise spectral density, respectively, T is temperature in degrees Kelvin, k is Boltzmann's constant, R_{FET} is the equivalent FET resistance and g_m is the small signal transconductance. The RMS noise current source in the frequency band [*f1, f2*] can be obtained from the spectral density:

$$I_{NB} = \sqrt{\int_{f_1}^{f_2} S_N \, df}$$

The simulated flip-flop output noise voltage spectral density curve is shown in Figure 5. This simulation was done with Cadence Spectre using the noise parameters supplied in the MOSIS device models for TSMC 350 nm technology. With a test frequency at 40 MHz, the noise band of interest is from 40 MHz to the cut off frequency at approximately 10 GHz. For this reason, the flicker noise was not included in Figure 5. The total simulated input-referred RMS noise is 1.2 mV.

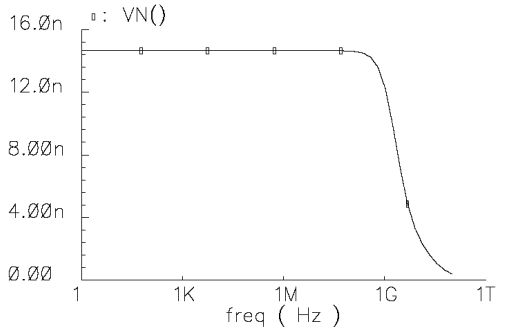

Figure 5. Flip-flop output noise simulation. Flicker noise is not included since only frequencies higher than 40 MHz are of interest.

2.3. Calibration Circuit

Although the flip-flop stochastic sensor achieves high gain, high resolution and noise immunity, it is extremely vulnerable to device mismatch. Due to the high gain, even a small mismatch will introduce a large offset. In order to correct the mismatch, two copies of the self-calibration circuit in Figure 6 are used to control the gate voltages of calibration pulldown transistors N5/N6 in the flip-flop.

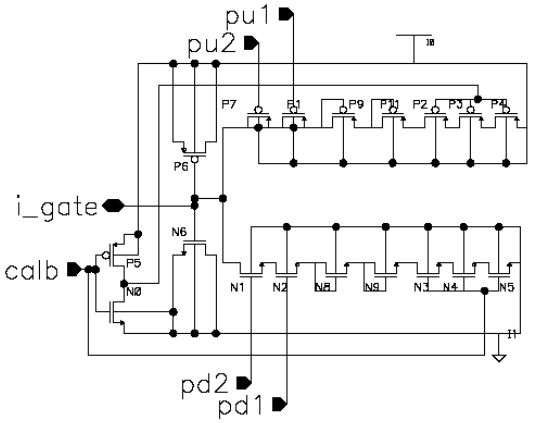

Figure 6. Calibration Circuit

The calibration circuit features high resolution, wide adjustment range and long holding time. Transistors P6/N6 act as a reservoir capacitor, with balanced gate oxide leakage. Transistors P1/P7 and N1/N2 form a pullup/pulldown charge pump controlled by non-overlapping clocks pu1/pu2 and pd1/pd2. To charge the reservoir capacitor, first P1 is pulsed to charge the P1/P7 parasitic junction capacitance and then P7 is pulsed to transfer the charge to P6/N6. Discharge is realized through the pulldown charge pump N1/N2 in a similar manner. Stack transistors P2/P3/P4 and N3/N4/N5 are shut off after calibration is completed and significantly reduce leakage [24] when holding the calibration voltage.

Two pairs of "diode-connected" transistors, P9/P11 and N8/N9 increase calibration resolution by limiting the calibration voltage range and acting as resistors to reduce the calibration voltage step size. They also reduce the calibration voltage drift rate.

Simulation and experiments show that the calibration voltages leak to an intermediate voltage when powered up, sufficient to turn on transistors N5/N6 in Figure 3. During calibration, each time the flip-flop makes a decision, the calibration circuit connected to the "1" side increases its calibration voltage and the circuit connected to the "0" side decreases its voltage, moving the flip-flop to a balanced state.

There are two primary challenges in the calibration circuit. The first is to achieve small voltage step size and the second is to minimize drift during measurement mode. A suitable charge pump capacitance ratio determines the step size while the drift issue can be alleviated by using high V_{TH} thick oxide devices and stacking them. The drift requirement of the calibration circuit is further reduced by using "digital chopping". In a standard chopper operational amplifier, the inputs are periodically shorted, and the observed output voltage difference stored on capacitors and then subtracted from the signal during sensing [25][26]. In our digital chopping approach, calibration periods and measurement periods are alternated. During a calibration period, the counters do not change, so the output value is not affected. By using shorter measurement periods, the drift requirements of the calibration circuit are relaxed, permitting use of smaller storage capacitors, and future leaky technologies. Frequent recalibration also compensates for temperature drift and low frequency external noise.

Circuit simulation of the drift rate was performed, with the results shown in Figure 7. The downward drift rate is 350 μV/10 ms and upward drift is 183 μV/10 ms. In practice, drift should be less than this since the calibration voltage should be close to $V_{DD}/2$ (1.65 V). Assuming a measurement period of 1000 clock cycles at 40 MHz (25 μs), the differential drift between two calibration circuits should be slightly more than 1 μV per measurement period. The equivalent input offset due to drift should be much less than this. Calibration drift is not a significant factor in 350 nm technology. In newer technologies, thick-oxide, high-V_{TH} devices in combination with higher clock frequencies (shorter measurement periods) can be utilized to minimize drift.

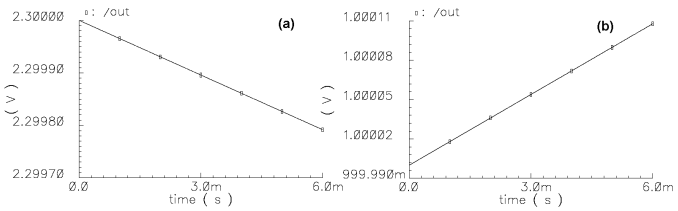

Figure 7. Circuit simulation of calibration drift at room temperature with 2.3 V initial voltage (a) and 1.0 V (b).

Due to the changing storage voltage and range-limiting diodes, the calibration step size changes with calibration voltage. Simulation of the pump up/down process is shown in

Figure 8. During pump up the calibration voltage tends to 'saturate' when it reaches 1.7 V, when the diodes go into their subthreshold region. In contrast, the pump down step size is varies less in the range of interest. The pump up process can be divided into two phases: coarse pumping (below 1.7 V) and fine tuning (above 1.7 V). In coarse pumping the average step size is 125 μV while in fine tuning it is 4 μV. The pump down process has an average step size of 31 μV. The simulated attainable pumping range is from 0.7 V to 2.11V. Beyond this range, the pump step size balances the drift in the corresponding clock cycle. The actual lower limit is less than 0.7 V, but the calibration transistor is cut off.

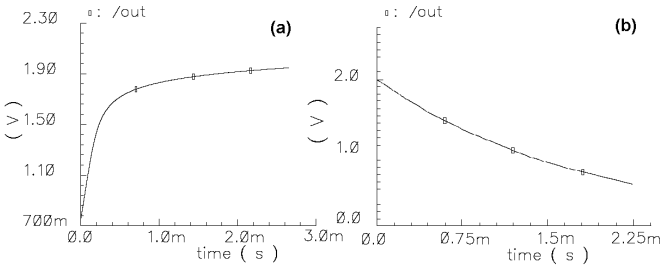

Figure 8. Simulation of calibration voltage pumping up (a) and pumping down (b).

2.4. Data Detector

In measurement mode, the data detector in Figure 9 passes the flip-flop results to the counter. In calibration mode, the data detector translates the flip-flop decision into calibration pump clocks. It produces non-overlapping pulse pairs pu1/pu2 and pd1/pd2, which pump up/down the calibration voltage through the calibration circuit.

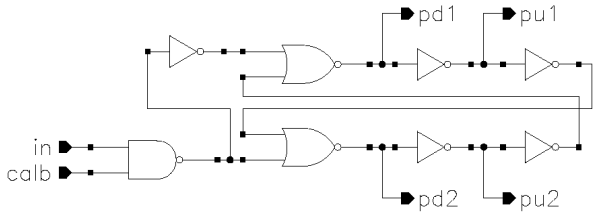

Figure 9. Data detector generates non-overlapping clocks.

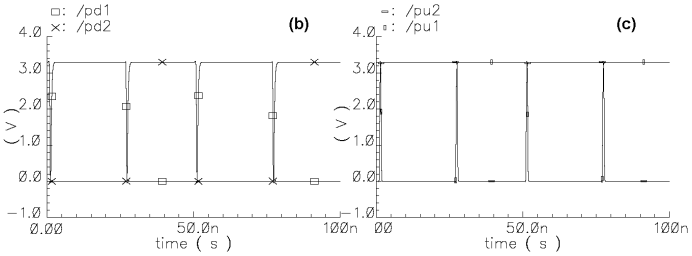

Figure 10. Simulated non-overlapping pump down (b) and pump up (c) pulses.

When the calibration enable signal CALB is held at 0, no calibration pulses will be generated. All pumping transistors and transistor stacks will be off to minimize calibration voltage drift. When CALB is 1, calibration pulses will be generated based on the flip-flop result. Simulation of the data detector is shown in Figure 10. A multiplexer is used to prevent flip-flop decisions from feeding the counter during calibration. This permits alternating calibration and measurement periods during "digital chopping" without disturbing the measurement result.

2.5. Counter/Scan Chain

Since stochastic analysis is a sampling process, a counter/scan chain was implemented in the BICS system to accumulate the result. In a production design, the counter would only be as large as necessary to hold the measurement result, log*N* bits for *N* measurement cycles. For the test chip design we included two 24-bit counts, one counting the "1" decisions, the other counting the "0" decisions, to aid in debug. A counter/scan chain cell is shown in Figure 11. In count mode (SCANB is high) it forms a toggle flip-flop. In scan mode (SCANB is low), pulldown transistors N9, N8/N5 and N6/N7 are shut off. Serial input T_1 is fed into the master stage through transmission gate P4/N10 to inverter P0/N0. Weak inverter P2/N2 provides feedback to make the master static. Transmission gate P3/N1 and inverter P1/N1 form the dynamic slave latch to output T. Q1/Q1B and Q2/Q2B are the non-overlapping scan clocks. In count mode, N9 is on, Q1 is low (Q1B is high), Q2 is high (Q2B is low), transmission gate P4/N10 is therefore off and transmission gate P3/N1 is on. The inputs T_1 and its inverse TB_1 control the pulldown paths N8/N5 and N6/N7. When N8/N5 is on, it pulls the input of inverter P0/N0 low, flipping the cell so that node B is high and outputs T low, and TB high. When N6/N7 is on, node A is high and node T high and TB low. Transistors N4 and N3 are used to store the previous state of A/B, and cause the cell to toggle on each input transition. The sequence of cells forms a ripple-carry counter. Since each bit flips at half the rate of the previous bit, the net active power dissipation of the counter is equivalent to two bits flipping every clock cycle. Circuit simulation shows that the counter is able to operate at several hundred megahertz. Simulation indicates there are small glitches in the toggle pulses, although no problems were found in using the cell in previous 1.5 μm and 180 nm designs. As a precaution, non-inverting buffers (not shown) were added to the T and TB output signals between each cell. These buffers can be removed in production sensors to save area.

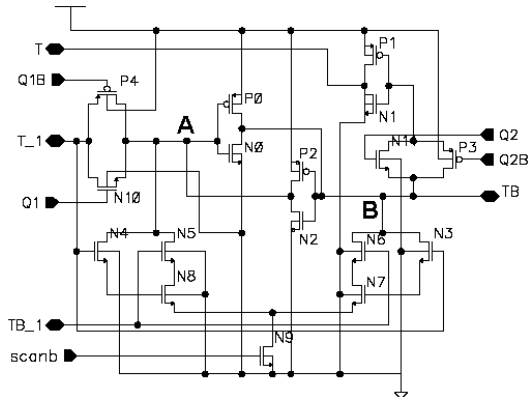

Figure 11. Counter/Scan Chain Cell.

2.6. BICS Operation and Controller Design

The operation of the proposed I_{DDQ} sensor consists of four different operation modes: scan-in, calibration, measurement and scan-out. In the scan-in mode, the counter is reset by scanning in zeros serially using the scan clocks, with SCANB

low. Similarly, the measurement results are scanned out using the counter/scan chain operating as a shift register. After scan-in, the external calibration signal (CALB) will be asserted along with the flip-flop clock to perform self-calibration. The normal measurement mode is initiated by removing CALB and applying flip-flop clocks. Measurement and calibration periods are interleaved to perform digital chopping. Scan-in and scan-out can be overlapped.

The tester interface can be simplified by having an on-chip controller generate the sequence of calibration and scan controls, flip-flop clock and Q1/Q2 clocks. A more ambitious approach would incorporate a complex controller which can implement a simple test algorithm such as ΔI_{DDQ} [27] or current ratio (CR) [28]. Controllers are implemented purely in digital logic and are small compared to the chip area and aggregate BICS area (assuming many BICSs). Since there is no concern about whether such controllers can be implemented in current and future technologies, they were not included on the 350 nm test chip.

3. Test Chip Measurement Results

The test chip was fabricated by MOSIS using TSMC 350 nm technology. The chip layout is shown in Figure 12. The test chip includes a full sensor (with two 24-bit counters) and its variations. It also includes individual components. The lower portion of the test chip contains MAGFET test structures, which are not discussed in this paper. The standard 40-pin ceramic DIP was used for packaging. Under a low-density layout, a full sensor with two counters is 83,490 μm^2. Removing one counter reduces the area to 53,850 μm^2. Shrinking the calibration capacitors and tightly packing the layout would reduce sensor area to 30,000 μm^2, permitting 33 sensors to use no more than 1% of a 1 cm^2 die.

The test fixture is based on a Xilinx FPGA Spartan system board D2E-DIO2. The FPGA was carefully programmed to generate test signals and store output results. An HP 1653B logic analyzer and an oscilloscope were also used to observe the output. A 40 MHz clock frequency was used for all measurements. This is the maximum clock rate of this test fixture.

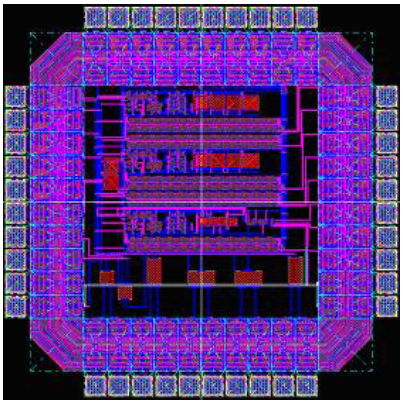

Figure 12. TSMC 350 nm test chip layout.

3.1. Calibration Step Size and Drift Measurement

The standalone calibration circuit was measured to determine the calibration charge pump voltage step size and the calibration voltage drift rate. Measurements show a calibration range from 330 mV to 2.03 V, compared to the simulated range of less than 0.7 V to 2.11 V. Since this range is primarily determined by transistor threshold voltages, and these are accurately characterized in the simulation models, there is good agreement between simulation and measurement.

As discussed earlier, the simulated calibration circuit pump up step size from simulation is 125 µV for the coarse phase and 4 µV for the fine tuning phase, and the average pump down step size is 31 µV. The two-phase characteristics of the pump up process were observed, with a measured coarse pump up step size of 232 µV and a fine tuning step size of 17 µV. The average pump down step size measured for the range 1.7 V down to 0.7 V was 87 µV. The measured step sizes are 2-4 times that of simulation.

The measured downward drift rate shown in Figure 13 is 770 µV/10 ms, from an initial voltage of 1.9 V. This is twice the simulated value. A slightly lower drift rate was observed for an initial voltage close to $V_{DD}/2$.

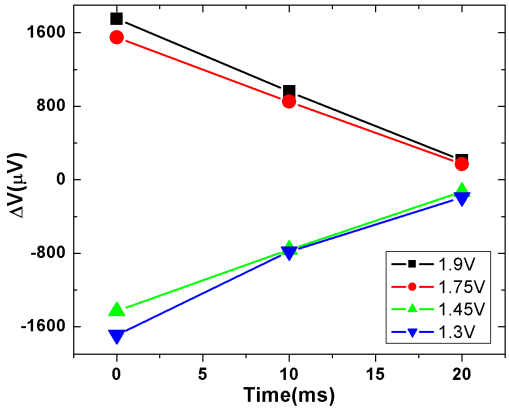

Figure 13. Measured calibration drift rate with different initial conditions. The y-axis is the amount of drift.

The calibration node voltage was measured on the standalone calibration circuit through an unbuffered (analog) pad. This results in the capacitance and leakage of the package and test fixture being included in the measurement. The leakage of the instrument probe is small enough to neglect. The combined capacitance from the pad, package, socket and instrument probe is approximately 20 pF, or about equal to that of the calibration reservoir capacitance. This means that the actual on-chip step sizes and drift rates are double their measured values. Therefore, the measured step size is 4-8 times the simulated value and the drift rate is four times its simulated value. Since MOSIS does not characterize device models for leakage, a large leakage error is not surprising. However, the MOSIS device large signal and parasitic capacitance values are accurately characterized. Since the measured calibration range is close to the simulated range, this suggests that models of the stack and diode-connected transistors are accurate.

The only possible explanation for the large step size is a problem with the pumping transistor control. If the non-overlapping pump clocks do in fact slightly overlap, this would explain the larger step size. However, a careful analysis of the data detector circuit using back-annotated netlists with run-specific electrical characterization data indicates that it should work correctly. Another possible

explanation is that V_{DD} and ground noise cause one pump transistor to turn partially on while the other is fully on. The pump transistors use normal V_{TH} devices. A glitch of 0.2-0.3V on the supply lines (fed through the data detector to the pump transistor gates) could produce enough leakage to explain the observed pump step size. However, such glitches were not observed on the supply lines at the package supply pins, and circuit power is low relative to supply impedance. Future designs will require a more robust pumping circuit.

3.2. Calibration Gain Measurement

The calibration gain was measured on the standalone flip-flop with external calibration voltages, using external counters to accumulate the results. The calibration gain was measured by shorting the flip-flop inputs to V_{DD} and slightly tweaking the calibration voltage. The calibration voltages used to balance the flip-flop were 1.907 V (on the "left" input) and 1.831 V (on the "right" input). The gain was then measured by manually adjusting the 1.907 V voltage up and down over a range of 10 mV with the other side fixed at 1.831 V and measuring the difference in up and down counter values. The results are shown in Figure 14. The input voltage is the difference from the initial balance point. A total of 1M (2^{20}) measurement cycles were used for each measurement, and the measurement repeated ten times and averaged. Over the calibration voltage range of ±2000 μV the flip-flop response is approximately linear, and so was used to estimate the gain of 253 counts/μV. This is equivalent to a gain of 1012 counts/μV for 4M (2^{22}) measurement cycles.

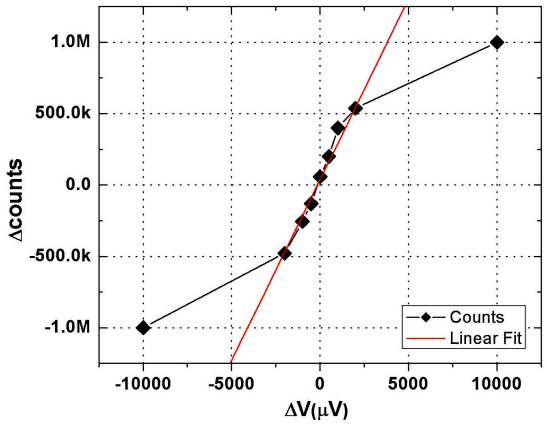

Figure 14. Calibration voltage gain in terms of differential counter value vs. change in calibration voltage away from the flip-flop balance point. The flip-flop inputs were shorted to V_{DD}, and a total of 1M (2^{20}) measurement cycles were used for each measurement.

3.3. Flip-Flop Mismatch and Gain Measurements

The standalone flip-flop was measured to determine its mismatch and gain. The flip-flop was designed with a common centroid layout and dummy transistors in order to minimize mismatch. Given the layout techniques used and transistor geometries, the primary source of mismatch is variation in transistor threshold voltages. The external calibration voltages were manually adjusted until the up and down counter values were approximately equal. The limited resolution of the manual adjustment left a small amount of offset. Since the two calibration voltages are independent, there are no unique calibration values. A set of values above and below $V_{DD}/2$ were used, as shown in Table 1. The flip-flop mismatch ranged from 30 mV to 150 mV, depending on the operating point of the calibration transistors. In the triode region, the mismatch compensation voltage was small due to the higher calibration device resistance. Note that in the self-calibration circuit one calibration voltage pumps up while the other pumps down, so the actual calibration voltage will be around $V_{DD}/2$, which suggests an expected nominal calibration voltage difference of about 50 mV for this particular flip-flop.

Table 1. Mismatch compensation under different calibration voltages.

Left (V)	2.524	2.171	1.939	1.673	1.211
Right (V)	2.374	2.079	1.856	1.621	1.181
Delta (mV)	150	92	83	52	30

The standalone flip-flop gain was measured by balancing the flip-flop at the three different calibration voltages, and measuring the gain curve for each of them for 4M measurement cycles. The gain curve is the plot of counter difference vs. differential input voltage. Ten measurements were taken for each input voltage. The results are shown in Figure 15 and Table 2. The flip-flop gain is slightly influenced by the calibration voltage. Increasing calibration voltage resulted in slightly lower gain, due to device operating points moving to a higher noise region. The highest gain of approximately 600 counts/μV is attained at the calibration voltage pair of 1.62 V/1.67 V, the pair closest to $V_{DD}/2$. Based on the gain curve, the estimated input-referred RMS voltage noise level is 1.5 mV, compared to the simulated value of 1.2 mV. The simulated value was measured as a steady-state value with the flip-flop operating point forced to the metastable point, and the real flip-flop devices transition between different operating regions, so this is good agreement between simulation and measurement.

Table 2. Flip-flop gain for different calibration bias.

Input (μV)	Calb A (1.62/1.67)	σ	Calb B (1.93/2.06)	σ	Calb C (2.53/2.37)	σ
1680	590016	5127	791814	4331	896306	5056
840	376154	4430	457708	3584	505212	4188
420	234822	3951	280196	4712	340628	3919
210	82138	4742	110704	4006	151768	4503
0	13166	3387	8798	3719	-7062	4154
-210	-83144	3509	-105172	4121	-171298	4321
-420	-208198	3592	-307908	3997	-279760	4681
-840	-391278	4636	-412010	4377	-510332	4844
-1680	-679390	4804	-731354	4970	-877390	4325

The flip-flop input gain of about 600 counts/μV for 4M cycles compares to a calibration gain of 1012 counts/μV. The calibration gain is 70% higher than the input gain because the calibration transistors have a longer channel length, and are at the bottom of the transistor stack, as shown in Figure 3. When the flip-flop is making a decision, both the input and calibration transistors operate in the linear region. The longer channel length of the calibration transistor means that it produces a larger resistance change per input voltage change than the input transistors, having a larger impact on flip-flop balance.

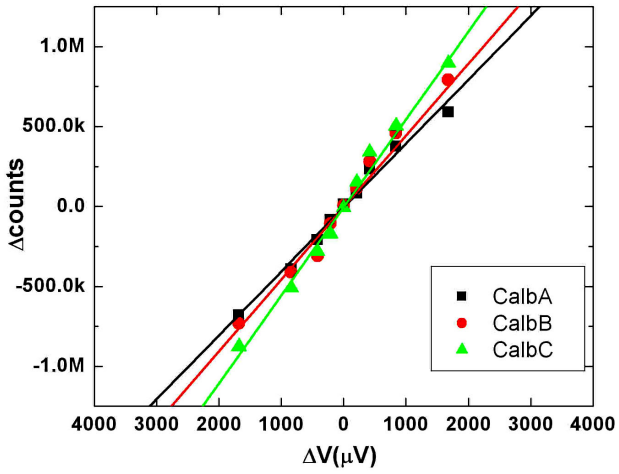

Figure 15. Standalone flip-flop gain under different calibration bias.

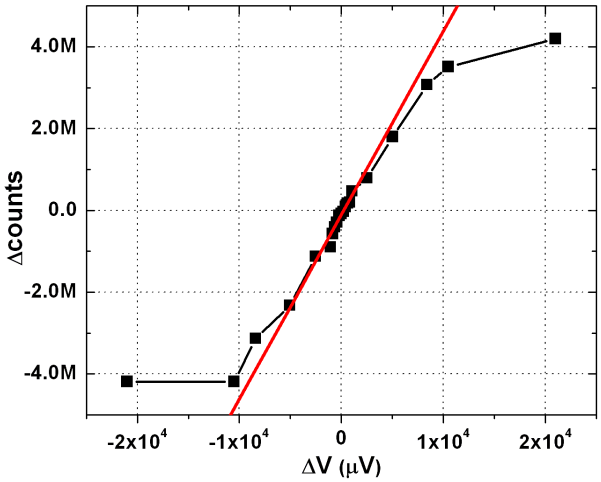

Figure 16. Transfer curve of the BICS using 4M measurement cycles, with 200 calibration cycles interleaved with 500 measurement cycles per period (mode B).

3.4. I_{DDQ} Sensor System Measurements

The entire sensor system in Figure 1 was measured. The input signal is taken from taps at two different locations 100 squares apart on a metal reference wire that emulates a V_{DD} line with a sheet resistance is 70 mΩ/□. So the sensing resistor is 7 Ω. This value is much larger than the expected design value of 100 mΩ in order to permit high resolution measurements.

Due to the leakage of 350 nm technology, it is not possible to measure the BICS transfer curve without using chopping. The curve shown in Figure 16 shows the difference in up and down counter values vs. sensor differential input voltage (set by adjusting the voltage on the reference wire). The curve was obtained using 4M measurement cycles at 40 MHz, with each measurement period of 500 measurement cycles following each calibration period of 200 calibration cycles. (This is referred to as Mode B below). The appropriate number of periods are interleaved to achieve the desired total number of measurement cycles, with the last measurement period being truncated as necessary. The corresponding data is listed in Table 3. Each point on the transfer curve is the average of 10 measurements. An effective input-referred RMS voltage noise level of 5 mV can be observed from the transfer curve. This suggests that self-calibration and the surrounding clocked circuitry (data detector, counter) add an additional 3.5 mV of noise.

A linear fitting around the origin indicates a sensor gain of 450 counts/μV, compared to 600 counts/μV in the standalone flip-flop. This difference is due to the different effective noise levels. The counter offset for a 0 V input corresponds to an input voltage offset of -194.4 μV.

Sampling theory predicts that the one-σ sampling noise (in terms of counter difference) for 4M measurement cycles should be 2048. The measured σ is about 3 times this value, and outside the 95% confidence range for ten samples when one considers that all samples are higher than predicted.

A possible explanation for the excess noise is a calibration sampling effect. As discussed above, the gain of the calibration circuit is approximately 1012 counts/μV of calibration voltage, so the observed σ of about 6000 is approximately the same as a variation in average differential calibration voltage of 6 μV between measurements. If 4M measurements are performed with 500 measurement cycles per measurement period, then there are 8388 calibration periods. The measurement cycles that follow a calibration period use the last calibration voltage throughout the measurement period, so only 8388 calibration voltage samples are used. The 95% confidence interval for 8388 samples is approximately ±1%. The measured differential step size ranges from 208 to 638 μV (accounting for the test fixture capacitance). A 1% variation about these values would explain the extra observed measurement variation. This was evaluated with further experiments.

Table 3. Counter difference and standard deviation under different measurement modes.

	Mode A		Mode B		Mode C	
ΔV (μV)	ΔCount	σ	ΔCount	σ	ΔCount	σ
21000	4.19E+6	0	4.19E+6	0	4.19E+6	0
10500	3.78E+6	7197	3.51E+6	6037	3.31E+6	8117
8400	3.31E+6	7562	3.07E+6	7332	2.77E+6	6090
5040	2.58E+6	6680	1.80E+6	6983	1.60E+6	6744
2520	1.39E+6	6911	7.90E+5	8129	979831	6938
1050	984486	9039	4.69E+5	6638	399078	7551
840	739154	8768	1.91E+5	7663	221070	7109
630	693340	5983	1.72E+5	8902	112453	8290
420	532473	6412	8.83E+4	7709	68303	7886
210	438343	7702	-3.58E+4	7006	45849	8366
0	217564	8751	-8.75E+4	5192	-17989	6334
-210	105930	8003	-1.34E+5	11208	-53890	7420
-420	94268	7610	-2.97E+5	9132	-137392	8637
-630	-18755	7149	-4.11E+5	6990	-311322	5275
-840	-73421	9785	-5.76E+5	7633	-445530	5993
-1050	-296011	6907	-8.98E+5	8991	-617672	8418
-2520	-716608	7759	-1.13E+6	7834	-1.23E+6	7525
-5040	-1.71E+6	8460	-2.33E+6	10033	-2.11E+6	9021
-8400	-2.56E+6	10715	-3.13E+6	6132	-3.34E+6	8792
-10500	-3.39E+6	11561	-4.19E+6	0	-3.98E+6	10056
-21000	-4.19E+6	0	-4.19E+6	0	-4.19E+6	0

The sensor behavior for different number of calibration cycles per calibration period was evaluated. We define modes A, B and C for 100, 200 and 1000 calibration cycles respectively, interleaved with 500 measurement cycles, and a total of 4M measurement cycles. The results are shown in Figure 17 and Table 3. Ten samples are taken for each input value for each mode. Mode C has the lowest offset and slightly higher gain than mode B. Mode A has poor offset and similar gain to mode B. The offset of modes A and B may be due to the initial calibration period, in which 100-200 cycles may not be enough to bring the flip-flop into initial calibration. Behavioral simulation indicates that initial calibration can take as long as 500 cycles. The variation in gain between the modes is within the 95% confidence interval, so any gain sensitivity to number of calibration cycles per period is small.

Behavioral simulation of the self-calibration process using Microsoft Excel was performed with the full range of measured calibration voltage step sizes and measured calibration gain. These simulations and an analytical model suggest that more calibration cycles per calibration period may increase the variance of the ending calibration voltage per period, effectively introducing noise and lowering gain. These simulations produce an effective calibration voltage RMS noise level of 0.6-1.2 mV and an input-referred noise level of 1-2 mV. This is well short of the measured noise that cannot be explained by measurement sampling. In addition, the predicted dependence on the number of calibration cycles per period does not match the data in Table 3. The simulation assumes equal up and down pump step sizes, and a linear flip-flop gain curve, which may explain its inaccuracy.

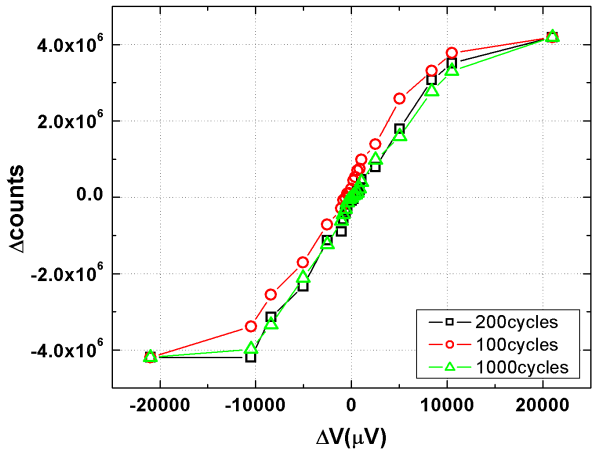

Figure 17. Comparison of three chopping modes with 100, 200 and 1000 calibration cycles, respectively. A total of 4M measurement cycles were used, with 500 measurement cycles per measurement period.

The behavioral simulation and sampling theory predict that using more calibration periods should reduce calibration sampling noise. Sampling theory also predicts that using more measurement cycles should reduce measurement sampling noise. Both the number of calibration periods and the number of measurement cycles can be increased by increasing the total number of measurement cycles while keeping the number of measurement cycles and calibration cycles per period fixed. This experiment was performed using 500 cycles per measurement period and 200 cycles per calibration period, with the total number of measurement cycles varying from 128K to 4M. The results are shown in Table 4. The relative σ of the counter differences increases by 4.33x for a 32x decrease in the number of measurement cycles. Sampling theory predicts a relative σ increase of 5.66x (√32). Given that σ is computed with ten samples, the difference between measurement and theory is within the 95% confidence interval. We can conclude that the counter behavior largely follows sampling theory, with calibration period sampling increasing the total σ by 30-50% over the measurement sampling alone. This indicates that the flip-flop is primarily affected by internal white noise and calibration noise that effectively acts as white noise.

Table 4. Counter difference and std. dev. for different total measurement cycles. All data was collected with 200 calibration cycles interleaved with 500 measurement cycles. Ten measurements were taken for each value.

	2^{17} Cycles		2^{19} Cycles		2^{21} Cycles		2^{22} Cycles	
ΔV (μV)	ΔCount	σ	ΔCount	σ	ΔCount	σ	ΔCount	σ
21000	131072	0	524288	0	2097152	0	4194300	0
10500	87139	639	476721	2325	1978751	4138	3511290	6037
5040	59301	904	229850	1728	1151406	3904	1798770	6983
1050	28641	921	90675	1514	290116	3774	469078	6638
630	23057	776	49188	1874	67115	4133	172453	8902
210	15902	853	13213	2007	9983	4017	-35849	7006
0	5315	752	3329	1644	-13071	4318	-87453	5192
-210	2385	694	-9789	1779	-53379	3692	-133890	11208
-630	-1438	813	-33080	1940	-133904	3869	-411322	6990
-1050	-9309	665	-87821	2021	-377683	3743	-898422	8991
-5040	-41033	840	-264487	1867	-1279213	4212	-2327600	10033
-10500	-76706	798	-407209	1993	-1807152	4635	-4194300	0
-21000	-112303	1103	-524288	0	-2097152	0	-4194300	0
Average		813		1881		4039		5998

In order to compare the gain as a function of number of total measurement cycles, all measurements were scaled to 4M cycles, as shown in Table 5, and drawn together in Figure 18. As can be seen, the flip-flop gain is relatively independent of the number of measurement cycles. This matches sampling theory. The exception is 128K cycles, which has lower gain and higher offset. But the size of the confidence interval makes it difficult to conclude that the 128K experiment has significantly different behavior. The data further indicates that the flip-flop internal white noise is relatively independent of the number of measurement cycles and calibration periods. As discussed above, this does not match the simple simulation and analytical model that was developed to describe calibration behavior.

Table 5. Scaled counter differences.

ΔV (μV)	128K	512K	2M	4M
21000	4194304	4194304	4194304	4194300
10500	2788448	3813768	3957502	3511290
5040	1897632	1838800	2302812	1798770
1050	916512	725400	580232	469078
630	737824	393504	134230	172453
210	508864	105704	19966	-35849
0	170080	26632	-26142	-87453
-210	76320	-78312	-106758	-133890
-630	-46016	-264640	-267808	-411322
-1050	-297888	-702568	-755366	-898422
-5040	-1313056	-2115896	-2558426	-2327600
-10500	-2454592	-3257672	-3614304	-4194300
-21000	-3593696	-4194304	-4194304	-4194300

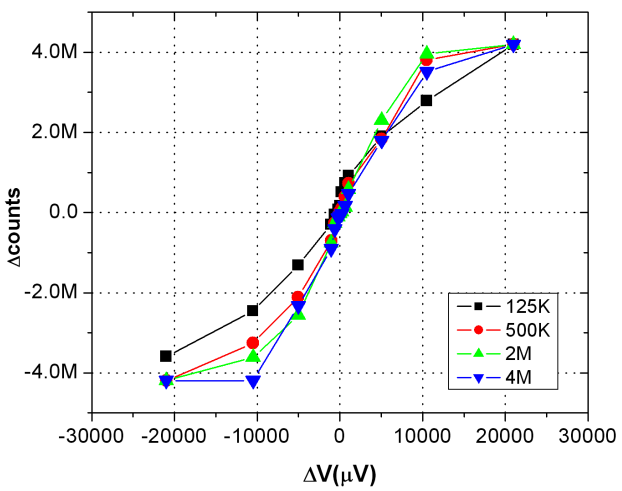

Figure 18. Flip-flop transfer curves for different total measurement cycles, normalized to 4M counts.

The length of the measurement period was varied, for a calibration period of 200 cycles and 4M total measurement cycles. The measurement period ranged from 50 to 500 cycles. This varies the number of calibration periods from 8388 to 83866. Sampling theory says that more calibration periods should reduce calibration noise and effectively increase sensor gain and reduce offset. The results are shown in Table 6 and Figure 19. The results indicate that there is only a very slight improvement in gain and variation by using fewer measurements per measurement period while keeping the total number of measurement cycles fixed. For 50 measurements per period, the gain was 659 counts/μV, compared to a gain of 650 counts/μV for 500 measurements per period. These differences are within the confidence interval of the measurements. The gain figures here are higher than those listed previously due to considering gain only near the origin. The results suggest that more calibration periods will not significantly reduce the effective calibration noise. The data shows that more calibration periods does significantly reduce the offset.

Table 6. Counter difference and std. dev. with different measurement cycles per measurement period, for 4M total measurement cycles, and 200 calibration cycles per calibration period.

	50		100		200		500	
ΔV (μV)	ΔCount	σ	ΔCount	σ	ΔCount	σ	ΔCount	σ
1050	635728	6926	518843	6522	672950	8122	469078	6638
840	366719	5874	330309	7481	397520	5713	191070	7663
630	247467	5638	172453	7931	210903	7090	172453	8902
420	69055	7110	71828	8005	114663	7509	88303	7709
210	33760	6865	21083	6592	70035	7336	-35849	7006
0	-18862	6397	-37453	6935	-33649	6596	-87453	5192
-210	-119438	7008	-83890	7120	-99806	6983	-133890	11208
-420	-183792	7041	-217392	7437	-197665	6837	-297392	9132
-630	-359081	6659	-391322	7589	-351322	8285	-411322	6990
-840	-472306	6347	-577012	8226	-466211	9014	-575530	7633
-1050	-749564	6582	-856641	7852	-703034	8998	-898422	8991

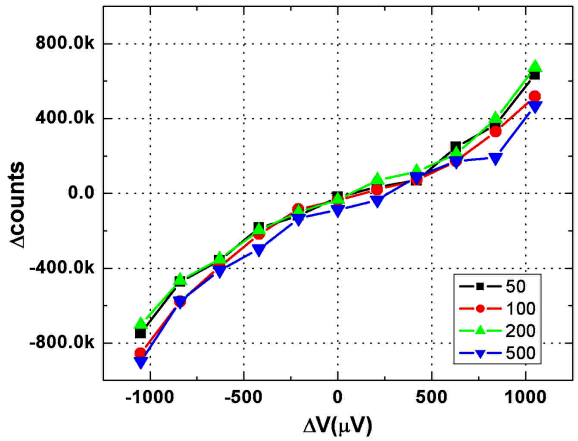

Figure 19. Flip-flop transfer curve for different number of measurement cycles per measurement period, for 4M total measurement cycles. Fewer cycles per measurement period means more calibration periods. 200 calibration cycles were used per calibration period.

4. Conclusions and Future Work

We have described a built-in current sensor that measures I_{DDQ} via the supply line voltage drop, and produces a digital result. A 350 nm test chip was fabricated and tested. Based on the measured results, the overall optimal performance of the BICS can be summarized as follows:

- **Gain** – 659 counts/μV for 4M measurement cycles with 50 cycles per measurement period and 200 cycles per calibration period.
- **Offset** – -18,862 counts or the equivalent of 28.6 μV. This corresponds to 286 μA if sensing a 100 mΩ resistor. This offset is not important if using a self-scaling testing approach such as ΔI_{DDQ}. In applications where a lower offset is required, a smaller number of measurement cycles per measurement period can be used.
- **Resolution** – The two-σ variation in measurement values is approximately 12,000 counts. This is the equivalent of 18.2 μV or 182 μA if sensing a 100 mΩ resistor. This corresponds to 0.4% of the dynamic range.
- **Dynamic Range** – The BICS is fairly linear over the input range of ±5 mV, or 50 mA. A larger range can be obtained by sensing a smaller resistance.
- **Measurement Time** – The test fixture limited the measurement clock to 40 MHz, even though in simulation the BICS can operate at several hundred megahertz. Using 50 measurement and 200 calibration cycles per period and 4M total measurement cycles takes 524 ms. Using 500 measurement and 200 calibration cycles per period and 1M total cycles slightly reduces the measurement resolution, but reduces the measurement time to 36.7 ms. Clocking the sensor at 400 MHz (e.g. using a locally generated clock) would reduce measurement time to 3.7 ms.
- **Power Dissipation** – The test chip structure did not permit measurement of an individual BICS, but the total power dissipation is small. During measurement the dissipation is equivalent to three flip-flops and a dozen gates switching each clock cycle. During calibration the

dissipation is half of this. During scan the power is similar to scan chains of the same size.

The experimental results indicate three primary areas for further sensor improvement. The first is the high flip-flop noise level, due to its high bandwidth. If the flip-flop cannot be clocked at higher speed, it can be loaded to reduce its corner frequency to about 100 MHz. This will reduce noise by 13x, with a corresponding increase in sensor resolution or reduction in measurement time. The second area is the low flip-flop input gain, which can be increased significantly by using a differential preamplifier. This should provide a corresponding increase in resolution. The third area to improve is the calibration step size, since this would reduce the number of calibration periods required and reduce the calibration noise. The challenge is achieving a small step size without increasing the calibration capacitor size. A new test chip incorporating these improvements is under development.

Acknowledgements

This research was funded in part by the Semiconductor Research Corporation under contract 2002-TJ-954. We would like to thank MOSIS for fabrication of the test chip under the MEP program.

References

[1] J. M. Soden and C. F. Hawkins, "IDDQ Testing and Defect Classes," IEEE Custom Int. Circuits Conf., 1995, pp. 633-642.

[2] K. Wallquist, "On the Effect of ISSQ Testing in Reducing Early Failure Rate," IEEE Int'l Test Conf., 1995, pp. 910-914.

[3] M. Sachdev, "Deep Sub-Micron IDDQ Testing: Issues and Solutions", European Design and Test Conf., 1997. ED&TC 97.

[4] T. W. Williams, R. Kapur, M. R. Mercer, R. H. Dennard and W. Maly, "IDDQ Test: Sensitivity Analysis of Scaling," IEEE Int'l Test Conf., Washington DC, 1996, pp. 786-792.

[5] Semiconductor Industries Association, International Technology Roadmap for Semiconductors, 2003.

[6] Kin, J. B., Hong, S. J. and Kim, J, "A CMOS Built-In Current Sensing Circuit," Int'l J. Electronics, Vol. 85, No.2, pp. 181-205, 1998.

[7] D. M. H. Walker, "Requirements for Practical IDDQ Testing of Deep submicron Circuits," IEEE Int'l Workshop on Defect Based Testing, Montreal, Canada, Apr. 2000, pp.15-20.

[8] J. Hurst, A. Singh, "A Differential Built-In Current Sensor Design for High Speed IDDQ Testing," VLSI Design Conf., Jan. 1995, pp. 419 - 423

[9] T. Calin, L. Anghel, M. Nicolaidis, "Built-In Current Sensor for IDDQ Testing in Deep Submicron CMOS," IEEE VLSI Test Symp., April 1999, pp.135 – 142

[10] M. Hashizume, Y. Miura, M. Ichimiya, T. Tamesada, K. Kinoshita, "A High Speed IDDQ Sensor for Low-Voltage ICs," IEEE Asian Test Symp., 1998, pp. 327 - 331

[11] C. Lu, C. Lee, J. Chen, "A Fast and Sensitive Built-In Current Sensor for IDDQ Testing," IEEE Int'l Workshop on IDDQ Testing, 1996, pp.56-58.

[12] K. Arabi, B. Kaminska, "Design and Realization of an Accurate Built-In Current Sensor for On-Line Power Dissipation Measurement and IDDQ Testing," IEEE Int'l Test Conf., 1997, pp.578-586.

[13] Y. Miura : "An IDDQ Sensor Circuit for Low-Voltage ICs," IEEE Int'l Test Conf., 1997, pp.938-947.

[14] T. Huang, M. Huang and K. Lee, "A High-Speed Low-Voltage Built-In Current Sensor," IEEE Int'l Workshop on IDDQ Testing, 1997, pp.90-94.

[15] H. Kim, D. M. H. Walker and D. Colby, "A Practical Built-In Current Sensor for IDDQ Testing," IEEE Int'l Testing Conf., 2001, pp. 405-414.

[16] J. P. M. van Lammeren, "ICCQ: A Test Method for Analog VLSI Based on Current Monitoring," IEEE Int'l Workshop on IDDQ Testing, Washington, DC, Nov. 1997, pp. 24-28.

[17] S. Sunter, "Private Communication," Industrial Test Challenges Meeting, 2002.

[18] B. Xue, D. M. H. Walker, "Built-in Current Sensor for IDDQ Testing," IEEE Int'l Workshop on Defect Based Testing, Apr. 2004, pp. 1-7.

[19] A. Prasad and D. M. H. Walker, "Chip Level Power Supply Partitioning for IDDQ Testing Using Built-In Current Sensors", IEEE Int'l Symp. on Defect and Fault Tolerance in VLSI Systems, Cambridge, MA, Nov. 2003. pp. 140-147.

[20] S. Hentschke, S. Rohrer, N. Reifschneider, "Stochastic Magnetic Field Micro-Sensor," IEEE ASIC Conf., 1996, pp. 11-14.

[21] J. Lin and M. Milkovic, "Performance Limitations of Stochastic Sensors," Midwest Symp. Circ. & Sys., vol. 1, 1992, pp. 408-411.

[22] W. J. Lian and S. Middelhoek, "Flip-Flop Sensors: A New Class of Silicon Sensors," Sensors and Actuators, No. 9, 1986, pp. 259-268.

[23] R. L. Geiger, P. E. Allen, N. R. Strader, "VLSI Design Techniques for Analog and Digital Circuits," McGraw-Hill, 1990.

[24] Z. Chen, M Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks," Int'l Symp. on Low Power Electronics and Design, 1998, pp. 239-244.

[25] E. Goldberg and J. Lehmann, "Stabilized DC Amplifier," U. S. Patent 2,684,999 1954.

[26] C. Enz, E. Vittoz, F. Krummenacher, "CMOS Chopper Amplifier," IEEE Journal of Solid-State Circuits, vol. 22 , no. 3 , Jun, 1987, pp. 335–342.

[27] C. Thibeault, "An Histogram Based Procedure for Current Testing of Active Defects," IEEE Intl. Test Conf., Oct. 1999, pp. 714-723.

[28] P. Maxwell et al., "Current Ratios: A Self-scaling Technique for Production IDDQ Testing," IEEE Intl. Test Conf., Atlantic City, NJ, Oct. 1999, pp. 738-746.