Wafer-level Spatial and Flush Delay Analysis for I_{DDQ} Estimation

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Abstract

Rising levels and spread in I_{DDQ} values render single threshold I_{DDQ} testing obsolete for high-performance chips for deep sub-micron technologies. Increased inter-die and intra-die variations cause unacceptable yield loss with a single pass/fail limit. Use of spatial information to estimate fault-free I_{DDQ} is investigated. Flush delay information is used to refine this estimate under varying process conditions. The analysis of SEMATECH test data is presented.

1. Introduction

I_{DDQ} testing is acknowledged to provide additional defect coverage [1]. It is shown to detect some latent defects that can lead to infant mortality [2,3,4,5]. However, shrinking transistor geometries and increased number of transistors elevate the background current and make it impossible to discriminate between normal high leakage and high leakage due to a defect. Process variations worsen the problem [6]. The overlap between faulty and fault-free I_{DDQ} distributions increases with each technology node [7, 8] causing more potential yield loss [9]. Several means have been proposed to solve this problem [10,11,12,13,14,15]. Some methods attempt to reduce the variance of fault-free I_{DDQ} so as to make faulty chips distinguishable [13]. One class of methods employs statistical means to uncover patterns in the data [11,14]. Yet another class of methods exploits correlation between I_{DDQ} and a second parameter like speed [16], temperature [17], and die position on a wafer [18,19].

In this paper we evaluate the combination of spatial information and flush delay to estimate fault-free I_{DDQ} in a manner similar to our previous work [19]. We use the SEMATECH data[1] for our analysis.

[1] This data comes from the Test thrust at SEMATECH, Project S-121 on Test Methods Evaluation. The conclusions drawn are our own and do not necessarily represent views of SEMATECH or its member companies.

This paper is organized as follows. Section 2 discusses the motivation. In section 3 we define our methodology. Section 4 includes some experimental results and section 5 draws conclusions.

2. Motivation

The variation in fault-free I_{DDQ} as well as increasing fault-free background current make it difficult to distinguish a faulty chip from a fault-free chip. This is illustrated by using I_{DDQ} values from the SEMATECH data. In the SEMATECH experiment four types of tests – functional, stuck-at, delay and I_{DDQ} test – were performed. I_{DDQ} was measured for 195 different vectors for each die. An I_{DDQ} pass/fail limit of 5 µA was used. We obtained median I_{DDQ} for all chips that passed all tests or failed only I_{DDQ} test at the wafer level and had maximum I_{DDQ} less than 100 µA. Figure 1 shows the histogram of median I_{DDQ} values of these 12187 chips. Note both axes have log scale and two orders of variation in I_{DDQ} is noticeable. Four levels of processing fluctuations are observed: lot-to-lot, wafer-to-wafer, inter-die (within-wafer) and intra-die (within-die) variations [20]. The spreads in I_{DDQ} at lot, wafer and die levels differ considerably as shown in Figure 2. This clearly indicates that any single I_{DDQ} pass/fail limit is not justifiable from a yield loss point of view.

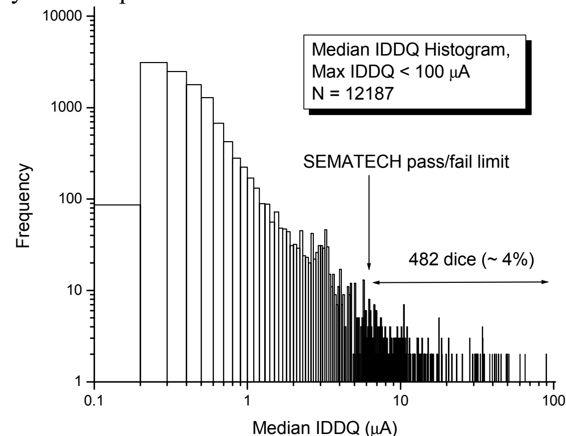

Figure 1: Median I_{DDQ} histogram

2.1 Relation between flush delay and I_{DDQ}

The leakage current or I_{DDQ} for gate to source voltage (V_{GS}) below threshold voltage (V_{TH}) is given by expression [21]:

$$I_{DS} = \mu C_{ox} \frac{W}{L_{eff}} V_t^2 e^{V_{GS} - V_{TH} / nV_t} (1 - e^{-V_{DS} / V_t}),$$

where μ is the electron carrier mobility, C_{ox} is the gate capacitance per unit area, W is the channel width, L_{eff} is the effective channel length, V_t is the thermal voltage, and *n* is a technology dependent parameter. The value of *n* is given by [22]:

$n = 1 + \frac{C_D}{C_{OX}}$,where C_D is the depletion layer capacitance per unit area. The leakage current and the effective channel length have an inverse relationship.

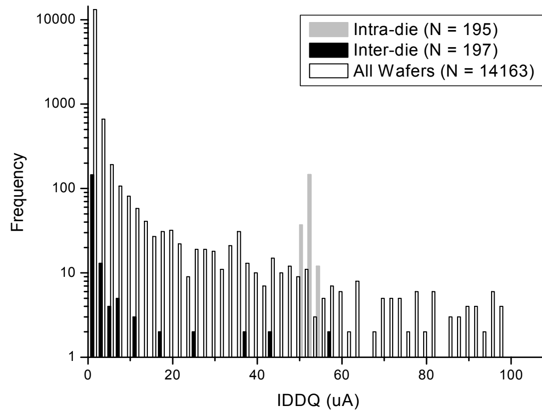

Figure 2: Inter-die and intra-die variation in I_{DDQ}

Figure 3 shows the histogram of flush delays for the 12187 all-pass/I_{DDQ}-only fail chips. Flush delay is obtained by turning on all scan clocks simultaneously, thus making the scan chain like a long wire with buffers and inverters [23]. The flush delay is the time it takes for a rising or falling transition to traverse the entire chain. For a full-scan design the scan chain practically traverses across the entire chip. Therefore, the flush delay is primarily determined by average device parameters [23],in particular Leff. Flush delay has been used for performance prediction for high-performance chips [24].

At a constant temperature and assuming low variance in other process parameters, since for most devices W >> L_{eff}, the variation in I_{DDQ} is mostly a function of variation in L_{eff} and V_{TH} [25]. However, V_{TH} also depends on L_{eff} among other parameters and the effect becomes pronounced as transistor geometries are scaled below 120 nm. Due to manufacturing variations, L_{eff} has a Normal distribution. The combined result of the dependence of V_{TH} on L_{eff} and variation in L_{eff}, is an exponential relationship between I_{DDQ} and L_{eff} [26].

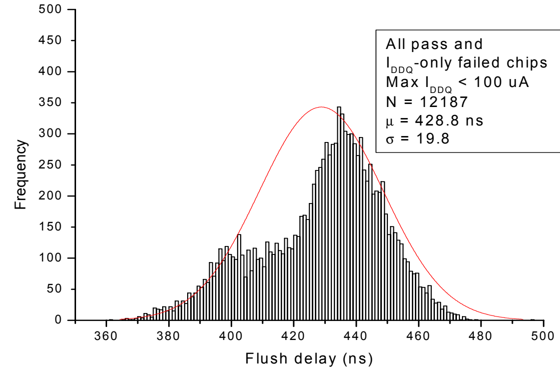

Figure 3: Flush delay histogram

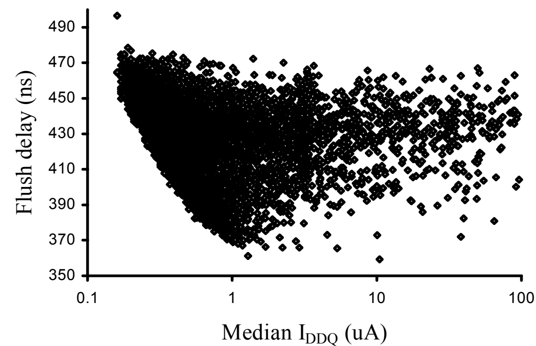

Figure 4: Flush delay against median I_{DDQ}

Flush delay is inversely proportional to L_{eff}. Thus transistors with smaller (longer) L_{eff} switch faster (slower). Smaller L_{eff} results in higher I_{DDQ}. Thus the relation between flush delay and I_{DDQ} is exponential. Figure 4 confirms this to be a general trend. A high degree of correlation can be observed between smaller I_{DDQ} and higher flush delay.

2.2 Spatial correlation

Prior work has shown that spatial correlation can be exploited for estimating fault-free I_{DDQ} [18,19,27]. This is based on a smooth change of process parameters across the wafer. Neighboring dice are subjected to similar manufacturing conditions, so their defect-free parameters are correlated. Thus, for a wafer region containing fault-free chips, across-chip variation in I_{DDQ} would be small. We examined several wafers for wafer-level spatial correlation between I_{DDQ} and flush delay. Figure 5 shows a typical surface plot for all dice on a wafer (wafer code: M855YXQ) that passed all the voltage tests. For each chip, the median I_{DDQ} value is plotted. Here the maximum median I_{DDQ} was limited to 50 μA. High-frequency

spikes indicate "spatial outliers". These chips have I_{DDQ} values much higher than that of neighboring chips. These chips are most likely to be defective and are potential candidates for burn-in. The grayscale plot for flush delays for this wafer is shown in Figure 6. The missing dice are indicated by blank squares. Some of the spatial outliers in Figure 5 exhibit smaller flush delay (i.e. fast chips) in Figure 6. However, some chips having high I_{DDQ} with respect to neighboring dice do not have smaller flush delays. These chips are likely to be defective. At wafer level different spatial patterns have been observed [27. In an Intel study for improving defect level the most influential neighboring dice patterns were studied [28]. For a die near the center of a wafer, the best predictors were dice surrounding it. For a die near the edge of a wafer, dice on or near the edge of the same wafer on the same side were highly correlated. However, for a die on the edge of a wafer, the best predictors were the same die positions on different wafers. We limit our analysis to eight neighboring dice.

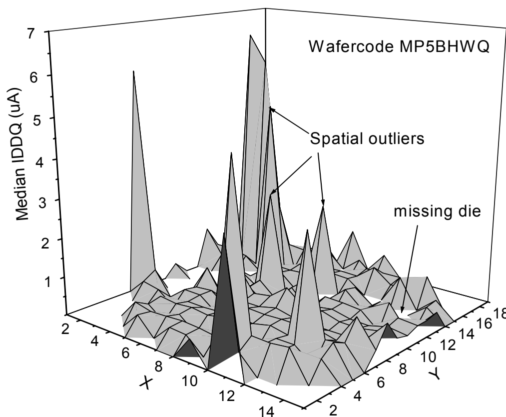

Figure 5: Wafer level spatial variation in I_{DDQ}

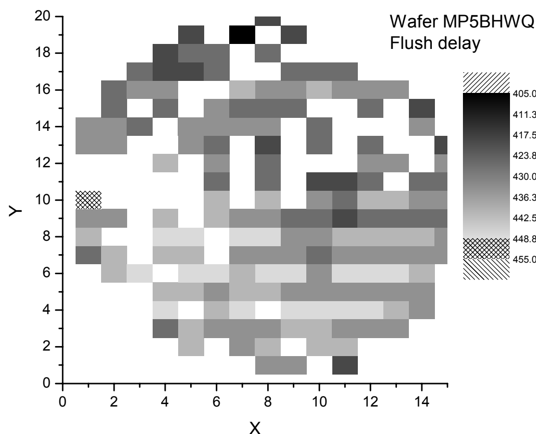

Figure 6: Grayscale plot for flush delay variation

The basic motivation for our analysis is to estimate chip-to-chip and wafer-to-wafer process variation from spatial I_{DDQ} and flush delay variation to obtain an upper bound on fault-free I_{DDQ}. This upper bound can then be used to determine appropriate pass/fail limits.

3. Methodology

We limit our data set to chips having six hours burn-in data (2660 chips). A large percentage of chips from SEMATECH data fail only I_{DDQ} test after burn-in. There is no clear oracle to define which of these chips are indeed defective, as all chips did not go through multiple burn-in cycles. It is necessary to eliminate gross outliers while forming a spatial estimate. To decide the outlier rejection limit, we obtained the histogram of wafer level minimum I_{DDQ} for these chips as shown in Figure 7. It reveals that a small percentage of chips (~2.5%) have *minimum* I_{DDQ} of more than 100 µA. Since minimum I_{DDQ} is mostly[2] an intrinsic component, such a high value is likely indicative of gross defect(s). So chips with I_{DDQ} above 100 µA are rejected even though they pass all voltage tests (1773 chips remain).

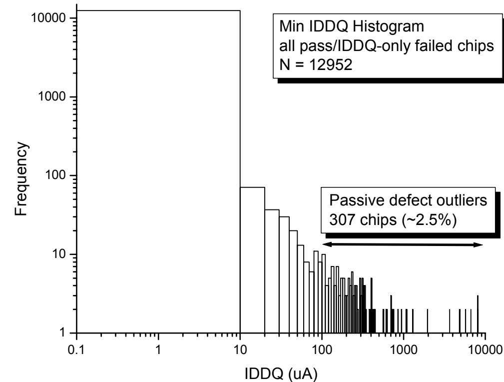

Figure 7: Wafer level minimum I_{DDQ} distribution

We obtain two estimates of I_{DDQ} for each vector for each die. The first estimate is obtained by using 3D linear regression between XY coordinates of the neighboring chips' I_{DDQ} as Z coordinate [19]. Only functional dice are used for plane formation. Since at least three dice are needed to define a plane, it is not possible to estimate I_{DDQ} for dice surrounded by more than five defective/missing chips. Such dice are excluded (187) from the analysis. The center die readings are not considered to avoid bias.

The second estimate is obtained by linear regression between neighboring chips' I_{DDQ} and flush delay values. Only functional dice are used in

[2] A part of minimum I_{DDQ} can stem from a subtle defect.

linear regression. This relationship is then used with the center die flush delay to predict the center die I_{DDQ}. The final estimate is the average of these two estimates. To account for random variations, a guard band of 20% is added to obtain an upper bound on estimated I_{DDQ} (I_E). Such analysis is performed for each vector.

The total leakage current (I_T) consists of two components: an intrinsic leakage component (I_L) and a defective component (I_D). If neighboring chips are fault-free, a high correlation between actual (I_T) and estimated I_{DDQ} (I_E) can be observed. However, defective component I_D depends on the nature and severity of the defect, input vector and several other factors. Thus for a defective chip actual values deviate considerably from the estimate. This is illustrated by a scatter plot of estimated and actual I_{DDQ} for a die as shown in Figure 8. For a defect-free chip, actual values would lie within the guard band obtained from the estimated values. If a defect exists, the elevated I_{DDQ} values form a cluster as shown. The approximate[3] defective component of the current is the residual value give by:

$$\delta = I_T - I_E$$

While a positive δ indicates a spatial outlier and a likely defective die, a negative δ could signify a good die in the bad neighborhood [29] or simply a test escape.

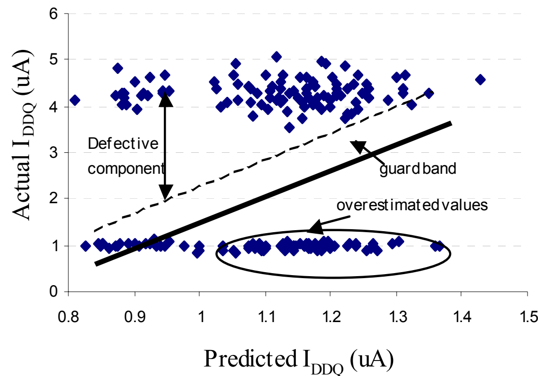

Figure 8: Correlating actual and estimated I_{DDQ}

Figure 9 shows the histogram of residual values for all chips (1773) for all 195 vectors. Approximately 80% of the residual values are within ± 25 µA. Therefore, any chip having δ > 25 µA is rejected. Any chip having δ < -25 µA is considered a reliability risk and is rejected. Since the 20% guard band is included, this is a relatively loose threshold.

4. Experimental Results

We performed wafer level analysis for all chips that either passed all tests or failed only I_{DDQ} test after removing outliers as explained earlier. A total of 1773 dice, of which 1044 passed all wafer tests and 729 failed only I_{DDQ} test, were analyzed. Out of 1044 dice, 1003 passed all tests after burn-in, 24 failed only I_{DDQ} test and 17 failed voltage test(s). Out of 729 I_{DDQ}-only fail dice, 524 failed only I_{DDQ} test after burn-in, 187 passed all tests and 18 failed voltage test(s). Since 5 µA did not necessarily imply a good manufacturing limit [30], all 729 I_{DDQ}-only fail dice are not necessarily defective.

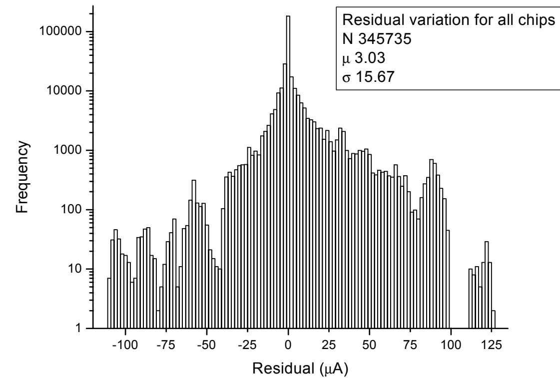

Figure 9: Residual variation across all chips

With I_{DDQ} plane fit alone, 1487 chips are accepted and 286 chips are rejected. Out of 1487 accepted chips, 1135 passed all tests after BI, 323 failed only I_{DDQ} test and 29 failed voltage test. Out of 286 rejected chips, 55 passed all tests after BI, 225 failed only I_{DDQ} test and 6 chips failed voltage test.

When flush delay information is combined with the I_{DDQ} plane estimate, 1538 chips are accepted and 235 chips are rejected. Out of 1538 accepted chips, 1176 passed all tests after BI, 332 failed only I_{DDQ} test and 30 failed voltage test. Out of 235 rejected chips, 14 passed all tests after BI, 216 failed only I_{DDQ} test and 5 chips failed voltage test.

Table 1 shows the distribution of chips accepted by both methods, rejected by either or both. In each category chips are divided according to their post BI result.

[3] The intrinsic leakage current component has vector-to-vector variation.

Table 1: Distribution of chips for two methods

Method	I_{DDQ}-only accept	I_{DDQ}-only reject	Post BI Result
I_{DDQ} + Flush delay accept	1132	44	Pass all
	302	30	Fail I_{DDQ}
	29	1	Voltage fail
I_{DDQ}+ Flush delay reject	3	11	Pass all
	21	195	Fail I_{DDQ}
	0	5	Voltage fail

When only I_{DDQ} information is used yield is 83.8%. If we assume all I_{DDQ}-only failed chips are fault-free (defective), defect level is 1.95% (23.67%). When flush delay information is combined and a chip is rejected only if rejected by both methods, yield is 88%. Assuming all I_{DDQ}-only failed chips are fault-free (defective), defect level becomes 1.92% (22.6%). Thus there is almost 5% improvement in yield and reduction in defect level. The reduction from 1.95% to 1.92% is not statistically significant considering the sample size. However, it can be argued that when flush delay information is combined with I_{DDQ}, increase in yield is not accompanied by increase in defect level.

When flush delay information is combined with I_{DDQ} information we obtain average of two estimates. For a chip that is rejected by I_{DDQ}-plane but accepted by the other method, the absolute residual value reduces. If the center die I_{DDQ} is in good agreement with flush delay prediction, such a die that is falsely rejected is moved to accepted bin. If the center die has high I_{DDQ} and high flush delay, residual increases and die remains in the reject bin.

5. Conclusions

It is increasingly difficult to distinguish between faulty and fault-free DSM chips using I_{DDQ} test alone. Traditional single threshold methods cause unjustifiable yield loss. It is possible to identify outliers by using wafer-level spatial information. However, to retain effectiveness of such outlier identification schemes for the next generation technologies it will be necessary to combine and correlate this information with multiple parameters. This paper presented a simple method where neighboring die I_{DDQ} was combined with flush delay information to estimate fault-free leakage current. Dice on the edge of a wafer are observed to show behavior that cannot be explained by spatial correlation-based scheme. By observing different spatial patterns on the wafer it is possible to find regions that are highly correlated [27, 28]. For stepper patterns in wafer level data, it might be beneficial to perform zonal analysis. A combination of wafer-median or similar method for outlier detection and multi-variant correlation would be needed for future technologies as each test technique loses its effectiveness in isolation. Similar to study reported in [28] it might be helpful to see whether dice from other wafers at the same XY location reveal any valuable information that can detect process defects.

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