Technology Scaling Issues of an I_{DDQ} Built-In Current Sensor

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Abstract

Analysis and comparison of 1.5 μm and 350 nm CMOS test chip results of a built-in current sensor design reveal several critical design issues. This paper includes a discussion of these issues. The success of the sensor design hinges on how these issues are addressed in order to achieve successful operation during technology scaling.

I. Introduction

As a supplement to functional test, quiescent current (I_{DDQ}) testing has been found to be an effective testing method in finding physical defects like gate oxide shorts and bridging faults. However, I_{DDQ} tests are facing challenges as technology advances. The built-in current sensor (BICS) approach has been widely investigated and proved to be a promising solution for future I_{DDQ} test. In our previous work we proposed a practical I_{DDQ} sensor design and fabricated test chips in 1.5 μm and 350 nm CMOS technology. Although test results showed that the basic sensor design works for both technologies, there are several issues need to be addressed for the sensor to scale with technology and find practical usage in current and future technologies. The two primary issues are storage of the calibration voltage and the signal to noise (SNR) ratio. Since the sensor stores a calibration voltage on a capacitor formed from MOSFET gate oxides, MOSFET transistor gate and subthreshold leakage become more and more of a concern. If not dealt with properly, they will significantly affect sensor performance or even void sensor functionality in future technologies. Sensor measurement time and resolution are quadratically dependent on SNR. Newer technologies have higher inherent bandwidths, which increase noise levels. Circuit bandwidths must be tailored to the test speed, in order to maximize SNR. Other design issues, including more robust signal preamplifier, sensor area reduction, sensor usage methodology and controller design, are also discussed in this paper.

II. Sensor Description

The block diagram of the BICS is shown in Figure 1. The detailed sensor design is described elsewhere [1][2][3]. The major BICS components are the flip-flop (FF) sensor, calibration circuit, and counter/scan chain. The BICS system works as follows. The signal, a small voltage drop from the supply line caused by leakage current, passes through the transmission circuit and into the stochastic sensor. The signal strength is decided by the supply line length and resistance. Ten squares of supply line will generate a 1 μV signal when the current is 10 μA and the sheet resistance is 10 mΩ/□. The stochastic sensor amplifies the small signal and resolves into either "1" or "0" in each clock cycle. The probability of the stochastic sensor resolving into each state is determined by the signal to noise ratio. The generated bit stream of "0" and "1" is then fed into the counter, where it is accumulated. A self-calibration circuit nulls out any flip-flop imbalance and layout mismatch when no input signal is present. The signal is removed for calibration by opening the transmission circuit and shorting the stochastic sensor inputs. The flip-flop sensor achieves high sensitivity by operating in the metastable region. It compares the input signal to random noise to determine which way to flip. The data detector converts this flip to a counter clock pulse. The counter value is the digital representation of the signal, so the stochastic sensor plus counter form an analog to digital converter (ADC). The counter value can then be scanned out. The stochastic method has two advantages: an ADC can be implemented in a small area using digital components, and it can measure a signal much smaller than the random noise.

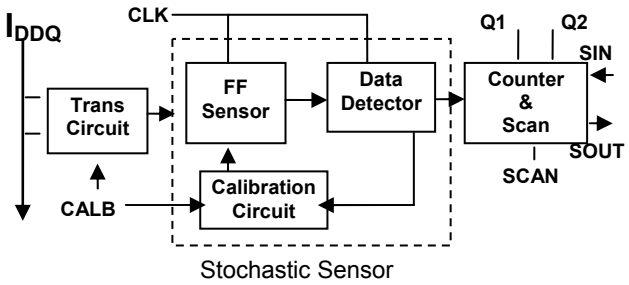

Figure 1. Block diagram of the I_{DDQ} Sensor.

III. Test Chip Measurement Results and Discussion

The test chip was fabricated by MOSIS using AMI 1.5 µm and TSMC 350 nm CMOS technologies. Both test chips used DIP 40 packaging and the same FPGA-based test fixture for experimentation and data collection. A summary of the test chip measurement results are listed in Table 1. It was found that the gain of the sensor system for both test chips is comparable, with the 1.5 µm test chip showing slightly higher gain. The transfer curves in both test chips have offset. The offset can be significantly improved by calibration, though it cannot be completely eliminated because of the limited calibration step size. However the offset problem is found to be alleviated for the 350 nm test chip when the step size is reduced. Based on the measured transfer curve and gain, the translated I_{DDQ} resolution is approximated 10 µA and 182 µA for the 1.5 µm and 350 nm test chip, respectively. The measured SNR is 1/800 for 1.5 µm and 1/1500 for 350 nm test chips. Besides the elevated internal noise, the calibration "noise" from digital chopping also contributes to the total noise observed. Dynamic range is basically the linear range of the transfer curve and the measured dynamic range is ±1 mV and ±5 mV respectively for the 1.5 µm and 350 nm test chips. Calibration step size directly affects the sensor accuracy and therefore several measures has been taken in the 350 nm test chip to reduce it, which includes diode connected transistors in the pump up/down paths to limit leakage current, and a larger pumping capacitance ratio. As a result the step size is reduced by 4-8 times. The calibration voltage drift rate is closely associated with the technology used, so the 350 nm test chip shows a leakage level approximately two orders of magnitude higher than the 1.5 µm technology. With worst-case circuit mismatch of several hundred mV, the calibration range is less of a concern compared to calibration step size and drift rate. Both test chips yield a wide calibration range of about 1.4-2.4 V. The sensor circuit scales directly with technology, except for the calibration reservoir capacitor MOSFETs, which are 50 by 50 µm in both technologies. Mismatch can be well controlled with certain layout techniques, but it is always unavoidable because of process variation. The measurements suggest the mismatch worsens as technology scales, which matches other published work. In the following sub-sections we will focus on the crucial issues that determine sensor success in current and future technologies.

Table 1. Comparison of the 1.5 µm and 350 nm test chip results

	1.5 µm	**0.35 µm**
Gain (with chopping)	950 counts/µV	659 counts/µV
Offset	200 µV	28.6 µV
Resolution	10 µA (60% confidence interval)	182 µA (95% confidence interval)
Measure SNR	1/800	1/1500
Dynamic Ranger	±1 mV	±5 mV
Calibration Step Size	850 µV (up) 640 µV (down)	232 µV (up) 87 µV (down)
Drift Rate	12 µV/20 ms	770 µV/10 ms
Calibration Range	0.7~3.1V	0.7~2.11V
Sensor Size	737,600 μm^2	83,490 μm^2
F/F Mismatch	7.2~49 mV	30~150 mV

Sensor System Gain

The stochastic sensor transfer curve of the 1.5 µm test chip is shown in Figure 2. The gain of the sensor is approximately 950 counts/µV, with an offset of about 200 µV, the result of a large calibration voltage step size. From the transfer curve, an effective noise level of about 800 µV can be estimated. As shown in Figure 3, the transfer curve of the 350 nm chip has a gain of 660 counts/µV. This difference is due to the higher effective noise

level of the 350 nm chip, estimated at 5 mV. Similar to the 1.5 µm chip, the 350 nm chip has an offset of approximately 190 µV for a 0 V input.

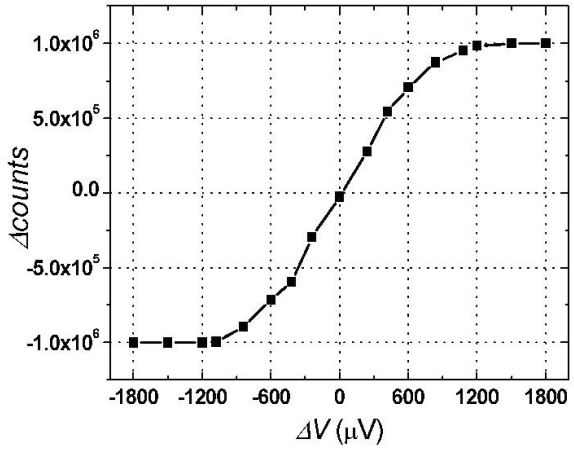

Figure 2. Measured stochastic sensor transfer curve of 1.5 µm test chip, in which 1M measurements are taken in chopping mode, i.e. 1000 measurements clocks are interleaved with 500 calibration clocks and repeat 1000 times.

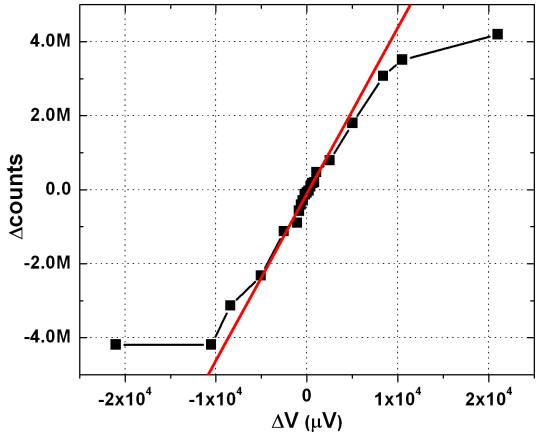

Figure 3. Transfer curve of the 350 nm test chip using 4M measurement cycles, with 200 calibration cycles interleaved with 500 measurement cycles per period.

Signal to Noise Ratio Improvement

Since the sensitivity is a function of the signal noise ratio (SNR) and the trend is worsening as technology advances, maintaining or improving SNR becomes more and more challenging. This can be done by either improving the signal strength or reducing the noise level. The latter can be achieved by reducing circuit bandwidth to the minimum needed for the flip-flop to operate at the clock rate. For example, the 350 nm design has a much higher bandwidth than the 1.5 µm design, but the clock rate of both is 40 MHz, so the extra bandwidth only contributes noise. Bandwidth can be readily controlled with flip-flop load capacitance or channel length. The signal strength can be improved with a preamplifier. Our flip-flop stochastic sensor design, though it has many advantages, has a limitation in that the input transistor gain is only half that of the calibration gain. In our next generation design, we will increase the input signal with a differential preamplifier that feeds each leg of the flip-flop. This both directly amplifies the signal and improves the transfer gain into the flip-flop differential voltage. This also allows us to reduce the calibration gain, which makes it less sensitive to calibration voltage drift due to capacitor leakage.

We have revised the flip-flop stochastic sensor to include a preamplifier based on a sense amplifier [4] which follows two principles. The design is shown in Figure 4. It is first a dynamic and differential logic style and therefore has only one switching event per cycle, and it is independent of the input value and sequence. Second, it guarantees the load capacitance has a constant value. The intrinsic capacitances at the differential input and output signals are symmetric and additionally it discharges and charges all the internal node capacitances through the pull down network. Circuit simulation results are shown in Figure 5. Compared with a sense amplifier, it has an essential difference. The two output nodes which are usually precharged by two clocked PMOS transistors (not shown) are

replaced by one clocked PMOS transistor P14 between the output nodes. Two schemes have been proposed with a small variation in that one has the shunting transistor N22 and one does not. The shunting transistor reduces power dissipation by reducing voltage swings. In our simulation of switching behavior and noise analysis, we favor the version without N22 since it outperforms the other in switching, while maintaining a lower noise level. Besides having a preamplifier, this stochastic sensor is faster than the previous design. During the precharge phase our previous stochastic sensor design discharged all nodes to GND and therefore it took longer to charge internal nodes and resolve to a flip-flop decision in the evaluation phase. In contrast, in the new design both output nodes are precharged to V_{DD}-|Vtp|-Vtn, reducing voltage swing. The circuit recycles charge during the evaluation phase, so is also lower power.

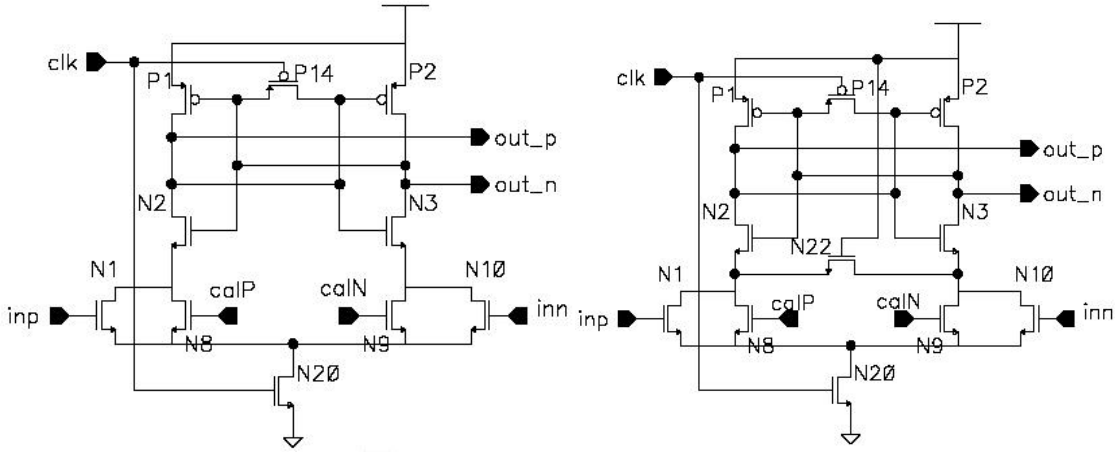

Figure 4. New flip-flop stochastic sensor with and without shunting NMOS transistor N22.

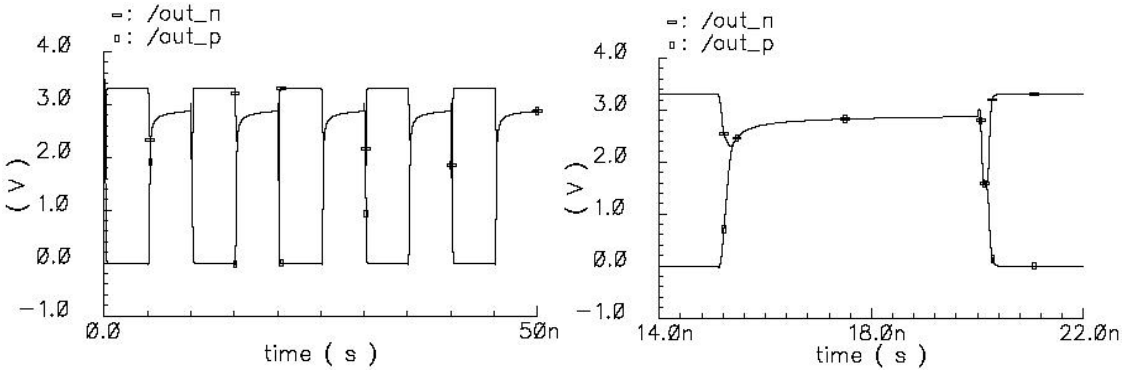

Figure 5. Simulated flip-flop waveform transients of the switching events and a single event zoom-in.

Calibration Drift Control

One of the core components in the sensor system is the flip-flop stochastic sensor, which operates in the metastable region and requires a precise adjustable calibration circuit to compensate for manufacturing mismatch to work properly. Hence, the calibration drift rate directly affects the sensor resolution and accuracy. The measured drift rate of the calibration circuit in the 1.5 μm chip is 12 μV per 20 ms, which is approximately an order of magnitude higher than the simulated results. The 350 nm test chip had a drift rate of 770 μV/10 ms, which is approximately twice the simulated value. This drift rate is two orders higher than that of the 1.5 μm test chip. This is due to elevated subthreshold leakage. In more advanced technology this issue will become more pronounced, due to gate leakage and band-to-band tunneling. The drift rate can be improved by increasing the size of the reservoir capacitor at the expense of chip area. Theoretical analysis shows that the charge pump will stop functioning when the technology intrinsic leakage achieves a certain level. The solution we are currently considering is using thicker oxide (high V_{TH}) devices to reduce leakage in the calibration circuitry and capacitor, and recalibrating more frequently to relax the drift requirements. Such recalibration requires more frequent switching of the calibration enable signal, which might reduce test speeds slightly.

Sensor Area Reduction

Since the test chips were pad-limited, no attempts were made to tightly-pack the sensor layout. The layout was also restricted to the first two metal layers to provide placement flexibility in using the sensor in a chip design. With this relatively loosely-packed layout, a full 350 nm sensor with two counters (up and down) is approximately 83,490 μm^2 using two 50×50 μm calibration reservoir capacitors on each side of the flip-flop. A production sensor will only need one counter, reducing the area to 53,850 μm^2. Shrinking the calibration capacitors (by using more frequent recalibration) and tightly packing the layout should cut the sensor area to approximately 30,000 μm^2, permitting 33 sensors to use no more than 1% of the area of a 1 cm^2 die. The sensor inputs can be multiplexed, at the expense of test time, to achieve further area reduction. We have shown how the sensor can be designed to measure all the V_{DD} pads of a Pentium 4 processor. We are also considering designing the flip-flop to contain an imbalance, so that only one side of the calibration circuit is needed, further reducing the sensor area.

BICS Sensor Usage Methodology and Controller Design

The tester interface can be simplified to realize a push button operation by having an on-chip controller generate the sequence of calibration and scan controls, flip-flop clock and Q1/Q2 clocks. The tester interface could then consist of two commands: CLEAR and MEASURE in which CLEAR would initialize the sensor while MEASURE would issue the sequence of calibration control and flip-flop clocks to perform the measurement. A more advanced controller can implement a simple test algorithm, for instance, ΔI_{DDQ} or Current Ratio. Controller designs are implemented purely in digital logic and are small compared to the chip area and aggregate BICS area (assuming many BICSs).

The operation of the proposed I_{DDQ} sensor consists of four different operation modes: scan-in, calibration, measurement and scan-out. In the scan-in mode, the counter is reset by scanning in zeros serially using the scan clocks, with SCANB low. Similarly, the measurement results are scanned out using the counter/scan chain operating as a shift register. After scan-in, the external calibration signal (CALB) will be asserted along with the flip-flop clock to perform self-calibration. The normal measurement mode is initiated by removing CALB and applying flip-flop clocks. Measurement and calibration are interleaved to perform digital chopping. Similarly, scan-in and scan-out can be overlapped.

The tester interface can be simplified by having an on-chip controller generate the sequence of calibration and scan controls, flip-flop clock and Q1/Q2 clocks. The tester interface could then consist of two commands: CLEAR and MEASURE. CLEAR would load zeros into the scan chains. MEASURE would issue the sequence of CALB and flip-flop clocks to perform the measurement. The MEASURE command could take parameters such as the total number of measurement cycles, and number of calibration and measurement cycles per period. After MEASURE, the tester could apply normal scan clocks, which would be converted into Q1/Q2 clocks by the controller, to read out the measurement values. The controller would feed in zeroes to reset the counters prior to the next measurement.

A more advanced controller can implement a simple test algorithm. For example, ΔI_{DDQ} can be implemented by scanning all sensor values into the controller, taking the difference between each measurement and the next, and remembering the max (and perhaps min) difference. The max difference could then be read out for a tester decision, either after each I_{DDQ} measurement, or after all measurements are completed. A current ratios test could be implemented by scanning out all sensor values, remembering the max and min values, which can then be read by the tester and divided to compute the current ratio. The NNR test method first computes the average of all I_{DDQ} vectors for each chip. This can be implemented by having the controller compute the sum of all sensor values for all vectors, which can then be read by the tester and divided by the total number of sensors and vectors. The assumption in CR and NNR that division is too expensive to implement in the controller and need only be done once.

Controller designs such as discussed above are implemented purely in digital logic and are small compared to the chip area and aggregate BICS area (assuming many BICSs). Since there is no concern about whether such controllers can be implemented in current and future technologies, they were not included on the 350 nm test chip.

Since the white noise spectral density is proportional to temperature, sensor gain falls with increasing temperature. Since temperature varies from sensor-to-sensor and over time, the gain must be calibrated if measurements are to be taken in terms of absolute I_{DDQ}. One solution is to bump up V_{DD}, measure the proportional increase in total chip I_{DDQ} and sensor values. If I_{DDQ} increased proportionally in all sensors, then the different sensor values indicate relative sensor gains. This also provides an indirect measurement of the temperature distribution across the chip. An alternative approach to gain calibration is to insert a switched current source into the V_{DD} line feeding each BICS sensor. This source would then provide a step increase in current, which would cause a corresponding increase in BICS counter value. Gain calibration becomes less important as statistical and self-scaling techniques such as NNR, CR and NCR are used for pass/fail determination.

IV. Conclusions

This paper compares the test results of a built-in current sensor fabricated in 350 nm and 1.5 μm CMOS technologies and discusses several technology scaling issues. A new stochastic sensor design incorporating a preamplifier has been proposed for better SNR over the previous design. The calibration circuit will use high V_{TH} devices for leakage reduction, achieving an acceptable drift rate. An on-chip controller design has been outlined for achieving tester push button operation. Several approaches for sensor area reduction were also discussed.

References

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