Requirements for Practical I_{DDQ} Testing of Deep Submicron Circuits

D. M. H. Walker
Dept. of Computer Science
Texas A&M University
College Station TX 77843-3112
Tel: (979) 862-4387
Fax: (979) 847-8578
E-mail: walker@cs.tamu.edu

Abstract

This paper describes the requirements that quiescent current (I_{DDQ}) testing must meet in order to continue being useful in the face of rising background currents. Using projections from the 1999 International Technology Roadmap for Semiconductors, several different techniques are evaluated to determine their usefulness in future technologies.

1. Introduction

Quiescent current (I_{DDQ}) testing has proven to be a very effective test screen for CMOS circuits. However MOSFET source-drain leakage currents (I_{off}) are rising rapidly with each technology generation, narrowing the difference between the I_{DDQ} levels of a faulty and fault-free circuit [1]. Projections from the 1999 International Technology Roadmap for Semiconductors (ITRS99) [2] relevant to I_{DDQ} testing of microprocessors (MPUs) are shown in Table 1. The roadmap assumes that gate dielectric leakage will be no more than 1% of I_{off} and so will be ignored here. This is due to the switch from silicon dioxide to a high-K dielectric such as zirconium oxide. Unlike previous editions of the roadmap, the 1999 edition describes both high performance and low power device needs. The low power devices are specified to have 1000 times lower I_{off} than the high performance devices. The ITRS99 specifies some figures, such as transistor per chip, for years between technology nodes. In order to keep Table 1 small, and simplify our analysis, we only show technology node years and linearly interpolate all figures specified for other years. The chip maximum I_{DDQ} entry is from ITRS99 Table 17. The total chip I_{DDQ} values are computed by assuming half the transistors are leaking, and the W/L of the transistors is 3. These are reasonable if one assumes that the leakage is dominated by SRAM arrays. The low power MPU is assumed to have the cost-performance MPU transistor count. The difference between our calculations and the ITRS99 Table 17 values are presumably due to different assumptions, such as transistor

Table 1. ITRS99 Technology Projections Relevant to IDDQ Testing

Year Technology Node	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
DRAM 1/2 Pitch (nm)	180	130	100	70	50	35
MPU Gate Length (nm)	140	85	65	45	32	22
Min logic Vdd (V) (desktop)	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6	0.3-0.6
Max I_{off} at 25°C (nA/um) (For min L device) high performance	5	10	20	40	80	160
Max I_{off} at 25°C (pA/um) (For min L device) low power	5	10	20	40	80	160
MPU cost-perf Mtransistors	24	71	190	539	1523	4308
MPU high-perf Mtransistors	110	331	882	2494	7043	19949
Max Total power and ground pads - MPU (2/3 of total pads)	1536	2018	2018	2560	2816	2944
Table 17 Chip Max IDDQ (mA)	5-30	30-150	150-400	400-1600	1600-8000	8000-20000
Chip IDDQ at 25°C (mA) MPU cost-perf	50	91	371	1455	5848	22746
Chip IDDQ at 25°C (μA) MPU low power	50	91	371	1455	5848	22746
Chip IDDQ at 25°C (mA) MPU high perf	231	422	1720	6732	27044	105330
Chip IDDQ Limit (μA) low power	67	83	111	167	200	333
Chip IDDQ Limit (mA) high perf	5000	8670	13300	18900	29000	30500
Chip IDDQ Limit (mA) cost-perf	5000	8670	13300	18900	29000	30500

count. The chip I_{DDQ} limits are computed using an approach similar to ITRS99 Table 28. The high performance and cost-performance MPU chip I_{DDQ} limit is computed as 10% of the heat sink power dissipation limit divided by the maximum supply voltage. The low power chip I_{DDQ} limit is computed as 100 μW divided by the minimum supply voltage. In contrast, the ITRS99 assumes a low-power leakage power limit of 10 μW, and in both high and low power cases specifies the leakage limit at 100°C, rather than the 25°C used here. The higher temperature increases leakage by about 100 times, so in both high performance and low power chips, the specified power limits can only be reached by using design approaches such as power supply switches to substantially reduce chip I_{DDQ}.

An additional difficulty in deep submicron technologies is that there is significant variation in effective channel length (L_{eff}) and transistor threshold voltage (V_T). The combination results in I_{DDQ} variations of an order of magnitude for good circuits. Combined with a higher background current, this makes it very difficult to distinguish faulty I_{DDQ} from process variation. One "solution" to this problem is to substantially reduce process variation [3]. However the ITRS99 already lists statistical process variation as a difficult challenge, so reducing the variation in advanced technologies from present levels is very unlikely.

In order to continue to be practical and useful, we believe that any I_{DDQ} testing approach must meet the following requirements:

- *Good fault coverage through multiple technology nodes*. Prior work has shown that most defective chips with anomalous I_{DDQ} have I_{DDQ} levels 5-100 μA or more above their nominal values [4][5][6][7]. As circuit performance increases, many of today's I_{DDQ}-only failures will cause delay faults, as indicated by recent failure analysis data [8]. To remain competitive with more effective delay testing, an I_{DDQ} test must screen out faults that cause elevated I_{DDQ}, but not a delay fault. The transistors assumed in Table 1 have an I_{on} of 100-315 μA in the 180 nm technology node, falling to 15-50 μA in the 35 nm technology node. We will assume that a fault that drains away 5% of the drive current from a device (e.g. a resistive bridge) is a reasonable detection threshold for faults that may not cause a delay fault but form a reliability hazard. This is a 5-16 μA defect today, falling to 0.8-2.6 μA in the 35 nm technology node. We will use a detection threshold of 2 μA to cover most of this range. The ITRS99 variation limit for L_{eff} is 20%. Combined with V_T variation this leads to as much as an order of magnitude variation in I_{DDQ} [9]. However much of this variation is deterministic, e.g. due to pattern density, and so can be calibrated for during testing. If we assume random local I_{DDQ} variations of up to 20%, then we must keep background I_{DDQ} levels to no more than 10 μA in order for the maximum random variation to equal the defect-generated current. Thus we assume that 10 μA must be the goal of schemes that attempt to reduce the background I_{DDQ} level.
- Circuit performance loss <1% and no significant increase in power supply noise due to any on-chip I_{DDQ} DFT circuitry. This is based on designer feedback.
- Chip area overhead <1% for on-chip I_{DDQ} DFT circuitry such as built-in current sensors (BICSs). This is based on MPU designer feedback.
- No special semiconductor processing steps. This would lead to unacceptable cost increase.
- Test time competitive with the best existing production I_{DDQ} test approaches (i.e. about 1 ms/vector). Faster test speeds are desirable.
- Ability to measure current level (not just pass/fail) and for BICSs the ability to measure current direction. Current levels are needed for limit-setting techniques such as current signatures [10]. The direction is required because in a mesh-type power supply network, process variation can cause the direction of nominal

Table 2. Supply Network Partitioning Requirements

Year	1999	2002	2005	2008	2011	2014
Technology Node	180 nm	130 nm	100 nm	70 nm	50 nm	35 nm
IDDQ/transistor (nA) high perf	2.1	2.55	3.9	5.4	7.68	10.56
IDDQ/transistor (pA) low power	2.1	2.55	3.9	5.4	7.68	10.56
Partition size (transistors) high perf	19048	15686	10256	7408	5208	1894
Partition size (transistors) cost-perf	19048	15686	10256	7408	5208	1894
Partition size (Ktransistors) low power	19048	15686	10256	7408	5208	1894
Partitions/chip MPU high perf	5.8K	21.1K	86K	337K	1.35M	10.5M
Partitions/chip MPU cost-perf	1260	4526	18.5K	72.8K	292K	2.3M
Partitions/chip MPU low power	2	5	19	73	292	2275
Max BICS Area (transistors) high perf	190	157	103	74	52	19
Max BICS Area (transistors) cost-perf	190	157	103	74	52	19
Max BICS Area (transistors) low power	190K	157K	103K	74K	52K	19K

current flow to change. The direction of current flow is also very useful for diagnosis.

In this paper we use these requirements to evaluate different proposed I_{DDQ} testing schemes to see how well they can be applied to the ITRS99 technology nodes. The goal is to identify future directions for I_{DDQ} testing.

Previous work on I_{DDQ} testing can be divided into reducing background I_{DDQ} levels and reducing signal variation. The goal of reducing the background current is to improve the signal-to-noise ratio of the measurement by making the background leakage and its noise smaller. The goal of reducing signal variation is to use measurement or signal processing techniques to cancel out process noise, and thus improve the signal-to-noise ratio. In Section 2 we evaluate some background reduction techniques. Then in Section 3 we evaluate some variance reduction techniques. Finally in Section 4 we conclude.

2. Reducing Background I_{DDQ}

A variety of approaches have been suggested to reduce background I_{DDQ} during I_{DDQ} measurements, including partitioning the power supply network, either externally or virtually with BICSs; lowering test temperatures; and increasing the backbias voltage [11][12]. Table 2 shows the requirements for partitioning the supply network to maintain a 10 μA background current within each partition. The same assumptions are used as in Table 1. The partition size is computed assuming half the devices are leaking and no additional design measures are taken to reduce leakage. Our assumption is that most design-based leakage reduction schemes will use power supply switches to power down inactive portions of the chip. But if the switched power partitions are larger than the supply partitions for I_{DDQ} testing, then switching does not reduce leakage since power must be applied during testing. The partition sizes in Table 2 clearly suggest this must be true for high performance and cost-performance MPUs. The I_{DDQ} partition sizes of the low power MPU are so large that power-switched partitions may be smaller, but to be conservative, we will assume they are larger. Overall leakage can also be reduced by techniques such as high-V_T devices on non-critical paths. However in a highly optimized circuit, many paths may be critical, so we assume that no such leakage reduction will occur.

The number of supply partitions per chip in Table 2 is the transistor count divided by the partition size, assuming the low power MPU has the same transistor count as the cost-performance MPU. The allowable BICS transistor count is computed as 1% of the partition size.

As can be seen in Table 2, the number of transistors within one supply partition is already very small for high-performance technologies, falling to less than 2000 transistors in the 35 nm technology node. The number of power supply partitions is relatively small for low power technologies, permitting external partitioning to reach the 10 μA leakage goals at least through the 100 nm technology node. The number of partitions required in high-performance technologies already greatly exceeds the number of power pads. In the 180 nm high-performance MPU, the leakage is projected to be 300 μA per power or ground pad. The number of power and ground pins on a package will be substantially fewer than the number of pads on the chip, so external partitioning becomes even less effective in I_{DDQ} testing of packaged parts.

BICSs avoid the pad or package pin limitation by logically partitioning the supply network within the chip. The only restriction is that every power or ground supply path must be monitored. This is relatively easy with a tree topology supply network, but more difficult with the mesh topology used in large chips. Most BICS approaches have one or more drawbacks: they cause unacceptable performance loss, they are limited in chip location, or they are incompatible with future technologies. Most BICSs insert a load device such as a diode, BJT, resistor, or MOSFET into the supply line, causing a 10-30% performance loss [13]. As noted below, high performance technologies are already starting to use silicon-on-insulator (SOI) substrates. These technologies are likely incompatible with diode or BJT load devices or require extra processing steps. It has been suggested [14] that the BICS can be used during wafer test, and then the sensor bypassed at package bond. This limits the sensor location to be near a supply pad. But the number of power pads is already insufficient for high-performance technologies. Area bonding also makes it difficult to bypass the sensor during the bonding process.

There are two published BICS approaches that do not cause a performance penalty and are flexible in sensor location. The first approach uses a differential amplifier to measure the voltage drop on a section of the supply line due to I_{DDQ} [15]. This approach was implemented in a production analog circuit using 24 sensors, which were multiplexed onto an analog bus for readout. The drawback of this approach is that it depends on a low peak-to-average ratio in supply current, and so is unsuitable for digital circuits. On-chip supply bypass capacitance reduces the peak current, but not sufficiently for this technique to be applied. The second published approach to non-invasive BICS is to use a Hall-effect sensor [16][17]. A current flowing in a wire generates a magnetic field that in turn causes a voltage differential across the Hall sensor. Since the Hall BICS indirectly measures the current, it does not affect circuit performance. As with sensing voltage supply line voltage drop, the central challenge in magnetic field sensors is the very small signal relative to background noise sources such as the Earth's magnetic field.

Even a working BICS is not a complete solution. It is doubtful that practical sensors can be realized within the size limits listed in Table 2 for high performance and cost-performance MPUs. If the sensor is to provide a value for readout on a scan chain, the scan chain alone is probably an order of magnitude too large. In combination with other techniques, such as those described below, the allowable sensor size might grow to a practical level. For low power MPUs, the allowable BICS size is large enough that area should not be a constraint to practical realizations.

Increasing the backbias voltage will increase the effective device V_T through the body effect and so reduce background I_{DDQ}. However this becomes less effective in future technologies since the gate dielectric breakdown voltage decreases, reducing the maximum backbias voltage that can be applied. In addition, it is not possible to change the backbias in SOI technology. The ITRS99 suggests SOI may come into widespread use for its performance advantages, and SOI-based products are already shipped in volume today.

Reducing the temperature will reduce I_{DDQ} [18]. Reducing the junction temperature from 25°C to -50°C reduces the leakage by 18 times, assuming a V_T of 0.3 V and a subthreshold slope of 80 mV/decade. But lowering the temperature becomes less effective at lower V_T values. Low temperature testing at -50°C is sufficient to reduce background leakage below 10 μA in low-power MPUs through the 100 nm technology node. Combined with external partitioning it can achieve this partition leakage through the 50 nm technology node, but is insufficient in the 35 nm node. However for cost-performance and high-performance MPUs a factor of 18 reduction is already insufficient, even combined with external partitioning. A low temperature test is also expensive and problematic.

3. Signal Variance Reduction

It is well known that the higher the I_{DDQ} level of a chip, the more likely it is to fail other tests, particularly after burn-in [19]. However it is also well-known that almost any reasonable I_{DDQ} limit results in test overkill [20] in that most failing parts will pass all other tests, even after burn-in. The result is that test engineers must balance the competing goals of improving product defect level and improving yield (minimizing overkill). Good chip I_{DDQ} levels vary due to circuit state, temperature, voltage, and process variation. These can cause a factor of four variation, primarily due to process variation [9]. The variation can be handled in two ways. The first is to attempt to set a pass/fail limit that achieves the desired defect level without significant yield loss. The second is to reduce the signal variation via measurement or signal processing techniques.

There are two basic approaches to the limit setting problem: empirical and model-based. In practice today the limits are set empirically by measuring the distribution of I_{DDQ} in a population of chips, and choosing a limit, such as 4 standard deviations above the mean, either one fixed limit, or a limit for each I_{DDQ} vector [5].

In a model-based approach to limit setting, a model of the circuit I_{DDQ} as a function of vector and environmental parameters is developed. Significant deviations above this value can be classified as faults. The advantage of a model-based approach is that pass/fail limits can be determined with very little or no production experience. This reduces test development costs in high volume manufacturing and is essential in low-volume products. Most model-based approaches to date have focused on the variation in I_{DDQ} from vector to vector [21][22][23], by evaluating the circuit state using a simulator, and using simple device equations. Process variation can also be included in the model [9]. The primary challenge in handling process variation is obtaining an estimate of the process parameters on a wafer or chip using simple electrical measurements.

Rather than setting pass/fail limits based on a model of the process, an alternative is to attempt to factor out the I_{DDQ} variation. A simple technique is to use the wafer median I_{DDQ} as an estimate of the nominal I_{DDQ} and adjust pass/fail limits relative to this value, along with a fixed limit to handle rogue lots. However the wafer median is only a good estimate of the nominal I_{DDQ} if most I_{DDQ} variation within the wafer is due to fixed process biases, rather than being random in nature. This is becoming less true with larger wafer and die sizes and smaller geometries. The wafer median approach can be refined using I_{DDQ} levels of neighboring die [24], in effect providing a local estimate of the nominal value. The drawback of these approaches is that the entire wafer must be tested before chip pass/fail can be determined. This is possible at wafer test with electronic wafer mapping. However at package test this is not possible either because lot history has been lost, or else because test handlers require disposition of a chip immediately following each package test.

An alternative approach to reduce noise is to use *current signatures* [10]. Current signatures combine the I_{DDQ} level from all vectors. This approach has the advantage that it searches for changes in I_{DDQ} over a set of vectors, thus factoring out process and environmental variations, and normal vector-to-vector variations. The disadvantage of current signatures is that they do not incorporate other available information, such as on-chip test structure measurements. In addition, they require that pass/fail determination wait until chip testing is completed.

A further improvement over current signatures is to perform *differential* I_{DDQ} testing [25][26]. Rather than the measurement directly, the absolute value of the difference

between a measurement and the previous measurement are recorded. These difference values have a smaller standard deviation than the original values. An analysis is then performed of the histogram to determine the pass/fail limit for the differential values. A factor of 39 gain in quality (escapes plus overkill) was achieved over I_{DDQ} measurements alone. As with current signatures, a complex analysis must be performed on all the test measurements before determining chip pass/fail.

A simple version of differential I_{DDQ} testing is to set upper and lower test limits around the first I_{DDQ} measurement. This serves as an estimate of the normal background leakage. If a measurement exceeds the upper limit, the chip is faulty. If a measurement falls below the lower limit, it means that the first measurement was faulty. This approach has the advantage that it stops on the first failure, and no complex analysis must be performed on the test results.

The *delta* I_{DDQ} technique is similar to the differential I_{DDQ} technique in that it measures differences between adjacent I_{DDQ} vectors [27]. In an SRAM, I_{DDQ} vectors had a mean of 2.3 mA and a 3 sigma limit of 6.6 mA. The delta I_{DDQ} measurements had a mean of 43 μA and 3 sigma limit of 3300 μA. In a Pentium the I_{DDQ} measurements had a mean of 4.5 mA and 3 sigma limit of 23 mA. The delta measurements had a mean of 4 μA and a 3 sigma limit of 62 μA. The much lower standard deviation permitted much tighter pass/fail limits. More than half the parts that passed functional and traditional I_{DDQ} tests but failed a 200 μA delta I_{DDQ} test also failed a 168 hour burn-in test. Note that 200 μA corresponds to almost 10 standard deviations, and so is a very loose limit. Compared to a single three-sigma limit, the delta technique results in a factor of 20 to 37 increase in resolution. In combination with external partitioning, this is adequate for the next several technology nodes. One open issue is whether smaller partitions will result in larger delta I_{DDQ} variation, due to less of an averaging affect.

Rather than comparing adjacent I_{DDQ} measurement values, the *current ratio* can be used [28][29]. This is the ratio between the minimum and maximum I_{DDQ} measurement values. The vectors on which these occur are determined during device characterization. From a set of devices, a relationship between the maximum and minimum I_{DDQ} value is determined as Max = Min*Slope+Intercept using linear regression with outliers (faulty chips) removed. The standard deviation of the residuals is also computed. The production test is done by measuring the minimum I_{DDQ} vector. An upper I_{DDQ} threshold for subsequent vectors is set as Tupper = Slope*Min_Measured+Intercept+3*Sigma_Residual. The lower limit is Tlower = Min_Measured-3*Sigma_Residual, clipped at zero. An absolute upper limit is also set based on chip transistor count. The advantage of this approach is that after the first measurement, all subsequent measurements have a fixed upper and lower limit. These can be programmed into the pin comparator logic, permitting high speed testing in conjunction with a load-board I_{DDQ} sensor. This technique results in a resolution improvement similar to delta I_{DDQ}.

The above approaches take differences or ratios in an attempt to remove I_{DDQ} variation caused by die-to-die process variation. An alternative approach is to take the original I_{DDQ} measurements and cluster chips based on multiple measurements, with chips within a cluster having similar behavior for all vectors [30][31]. This in effect also removes process variation, and results in an improvement in measurement resolution.

An alternative to quiescent current measurements is to take transient current or I_{DDT} measurements. The advantages of dynamic measurements are that the steady-state value is factored out, a dynamic measurement can detect faults that are not detectable with a low-speed test, and I_{DDT} tests can be applied at high speed. Most proposed I_{DDT} testing approaches [32] attempt to take multiple current measurements during a clock cycle. In order to improve the signal-to-noise ratio, the measurement may have to be repeated thousands of times. This can be avoided by using an inductive current measurement probe, and measuring the undershoot on the probe output [33]. This has the advantage of being a relatively low frequency measurement, and so less sensitive to timing. In an experiment on a 186K gate chip and 123 vectors, this approach achieved the same coverage as differential I_{DDQ} testing.

A dynamic measurement approach that also avoids the need for a high-speed measurement is the energy consumption ratio (ECR) [34]. Each fault site is targeted with a pair of vectors, an energy test pair and a benchmark pair. The energy pair is chosen so as to maximize the average current if a fault is present. The benchmark pair is chosen so that the current is not affected by the fault. The ECR is the ratio of the test pair average current to the benchmark pair average current. Use of the ratio minimizes the impact of process variation, improving measurement resolution.

The summary of the signal variation reduction techniques is that they are capable of a factor of about 40 or better improvement in effective measurement resolution. In terms of the ITRS99, this is adequate for all nodes of the low power MPU, when design-based power reduction techniques are used, but is already inadequate for cost-performance and high performance MPUs.

4. Conclusions

The conclusions of the above analysis are that with the exception of low-power MPUs, no one technique is

sufficient to reach the 10 μA background leakage goal for all technology nodes. Individual techniques such as BICSs can handle cost-performance and high-performance MPUs for several generations, but beyond that techniques must be used in combination. A factor of 20-40 improvement in resolution from variance reduction techniques, in combination with BICSs, should handle all technology nodes. If SOI technologies become popular, there appears to be little future in backbiasing techniques. Given the expense of a low temperature test, and its declining effectiveness with decreasing V_T, variance reduction techniques are much preferred. I_{DDQ} testing of cost-performance and high performance MPUs appears infeasible without BICSs.

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